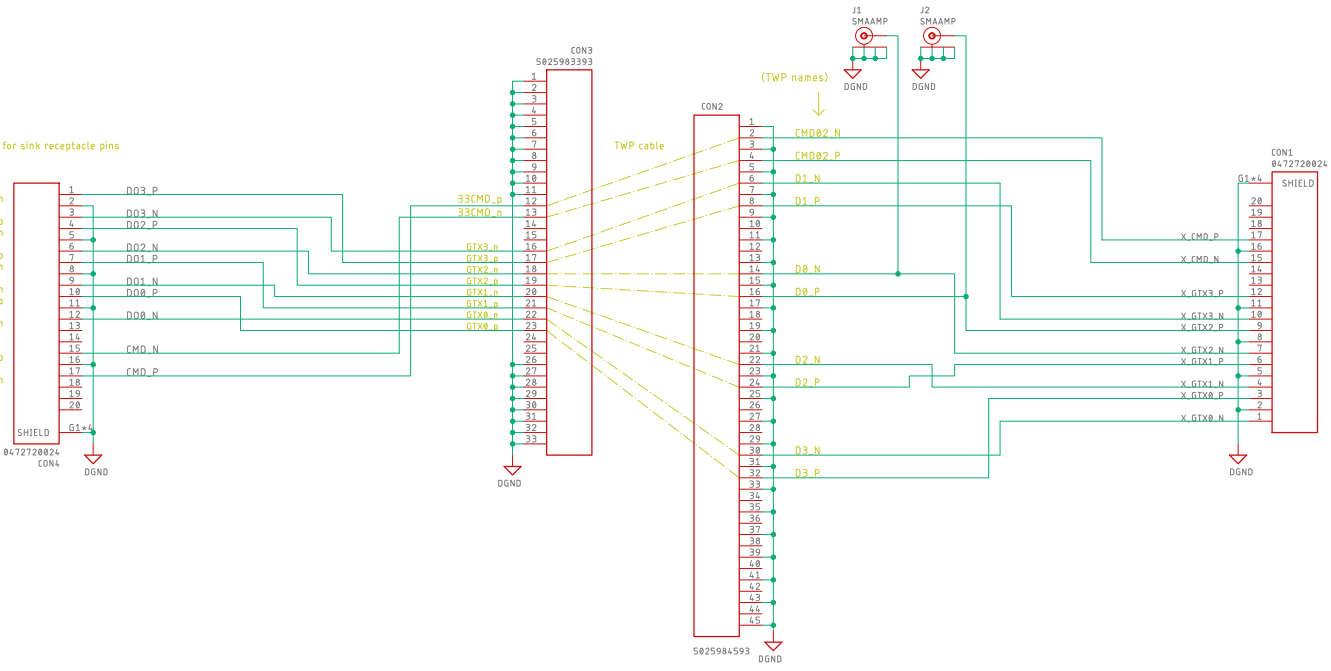
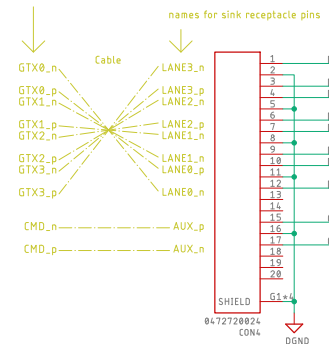


REVISION RECORD			
REV	ECO	APPROVED	DATE
A	original		
B.4	Removed caps, Revised interconnect		
C	add 1SMA to look at data pair		

B, B.1, B.2 and B.3 worked through changes required. B.4 is desired layout.

Signal names as found on RD53A_SCC_Rev0.2.c schematic
 Note we have boards labeled Rev 0.2d but schematic is 0.2c. Looking at a Rev 1.0 schematic the names and order remain the same so we are assuming this is the correct pin out.



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Project: eLINK Type I Cable to Display Port Adapter
 Sponsor: A. Bean
 Date: 9/2/2021 9:07 AM
 Sheet: 1/1

