

Experimental techniques in high-energy nuclear and particle physics

“Dottorato di Ricerca in Ingegneria dell’Informazione”

LECTURE 8.

Prof. Rino Castaldi

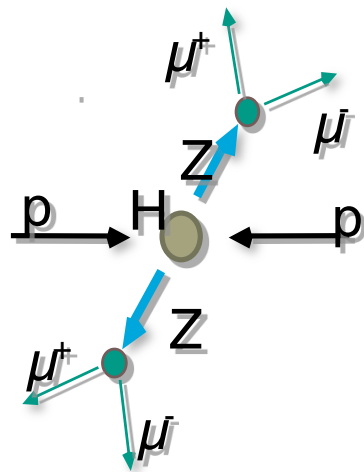
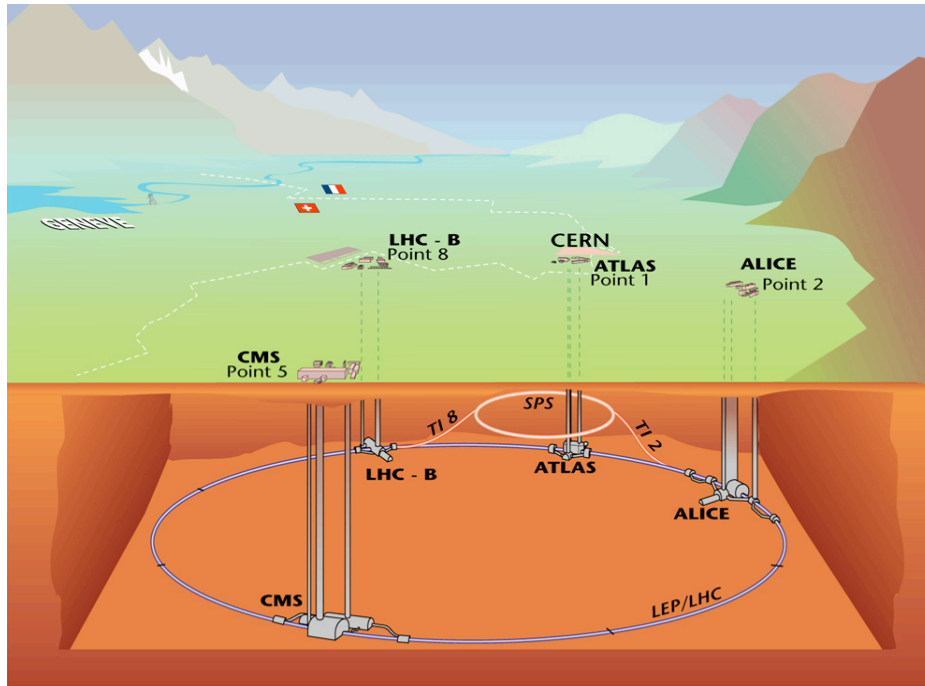
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The CERN Large Hadron Collider



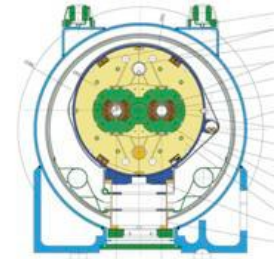
9300 Superconductor magnets
 1232 Dipoles (15m, 1.9°K) 8.4Tesla 11700 A
 448 Main Quads, 6618 Correctors.
 Circonference 26.7 km



• Higgs :
 Clarify the origin of the
 spontaneous symmetry-
 breaking Standard Model
 (-> Higgs, SUSY)

- New forces (symmetries)
 - New particles
 - Super symmetries
 - Substructures
-

LHC DIPOLE : STANDARD CROSS-SECTION





Signal and background $\rightarrow \mathcal{L}=10^{34} \text{ cm}^{-2}\text{s}^{-1}$

Event rate = $\mathcal{L}\sigma\text{Br}$

Cross sections for various physics processes vary over many orders of magnitude

Higgs ($600 \text{ GeV}/c^2$): $1\text{pb} @10^{34} \rightarrow 10^{-2} \text{ Hz}$

Higgs ($100 \text{ GeV}/c^2$): $10\text{pb} @10^{34} \rightarrow 0.1 \text{ Hz}$

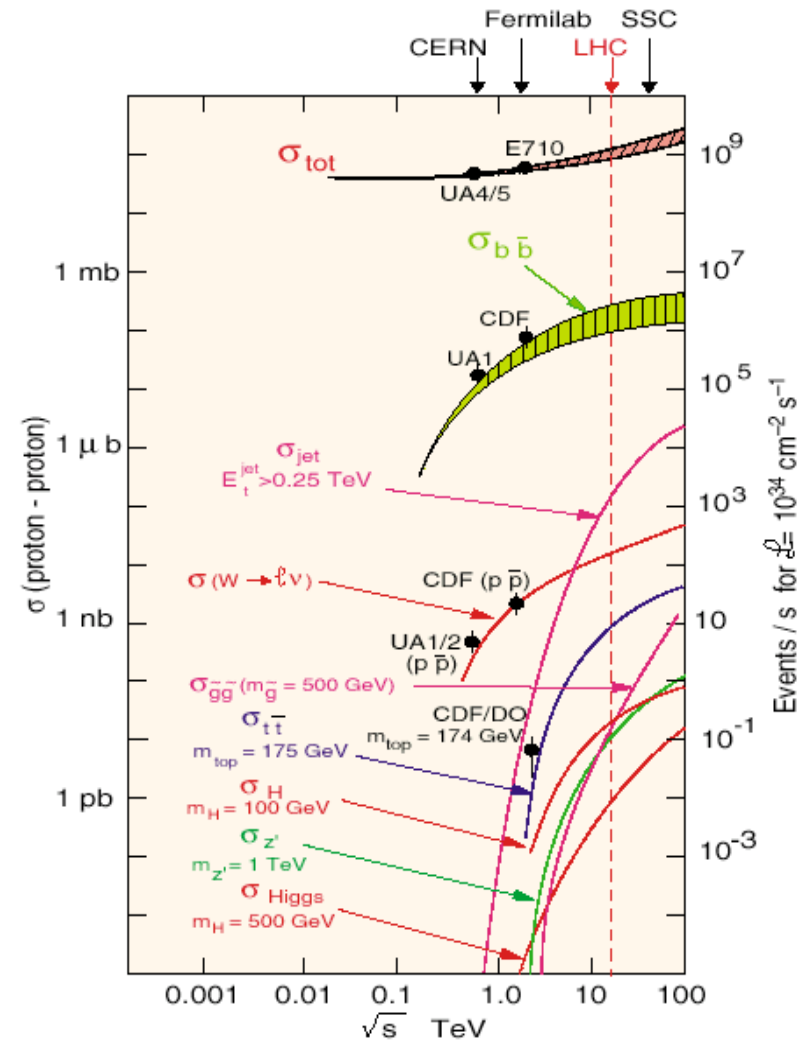
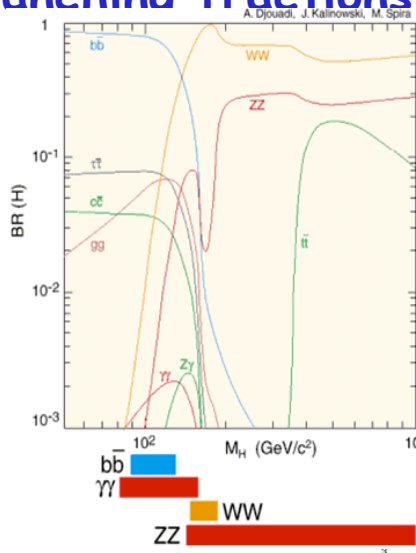
$t\bar{t}$ production: $\rightarrow 10 \text{ Hz}$

$W \rightarrow \ell\nu$: $\rightarrow 10^2 \text{ Hz}$

Inelastic: $\rightarrow 10^9 \text{ Hz}$

Selection needed: $1:10^{10-11}$

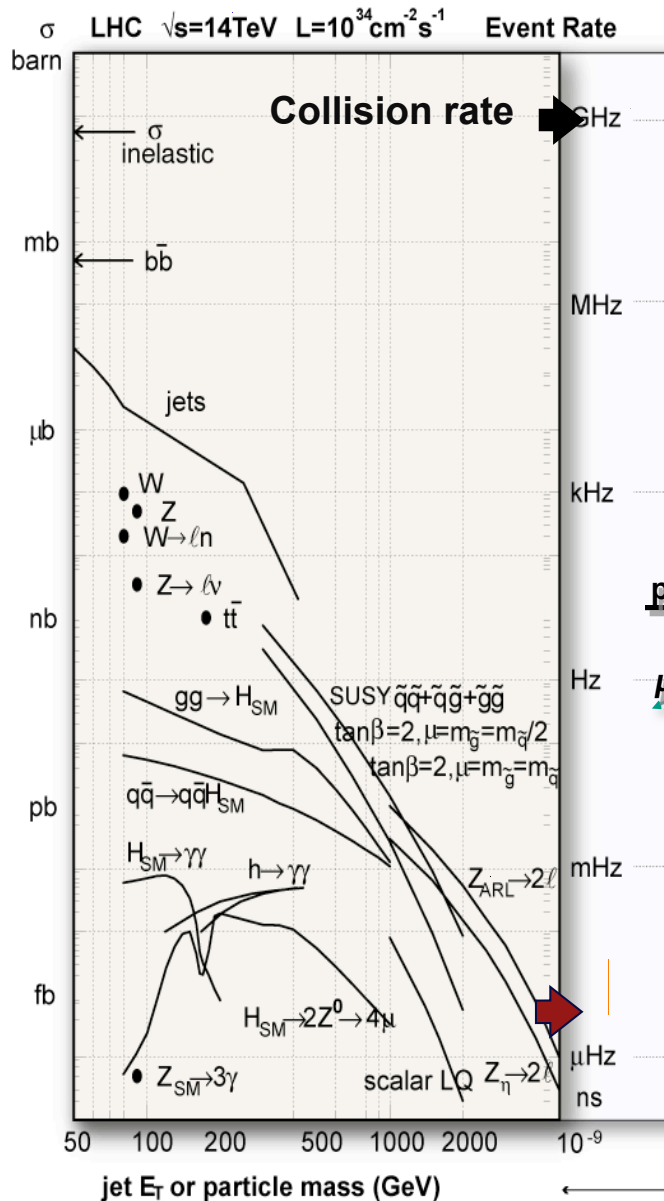
Before branching fractions...



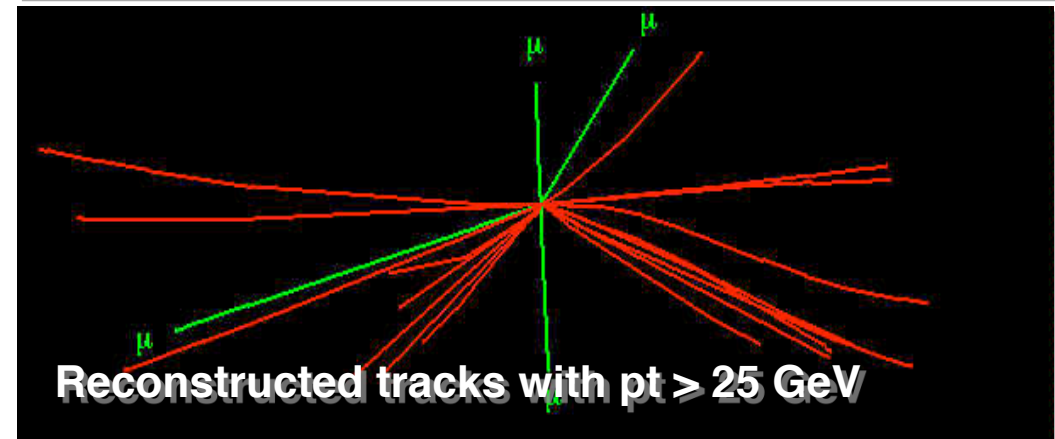
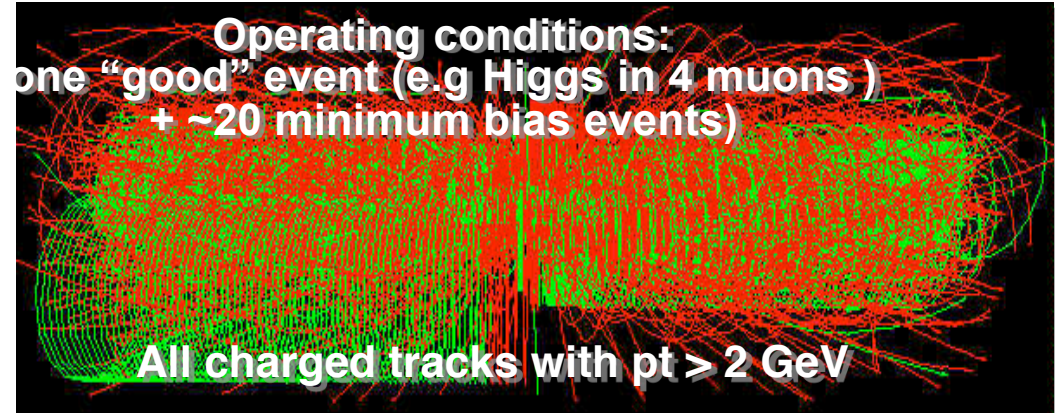
\Rightarrow Needle in a Hay Stack



Data detection and data filtering



Operating conditions:
one "good" event (e.g Higgs in 4 muons)
+ ~20 minimum bias events)



Detector granularity

$\sim 10^8$ cells

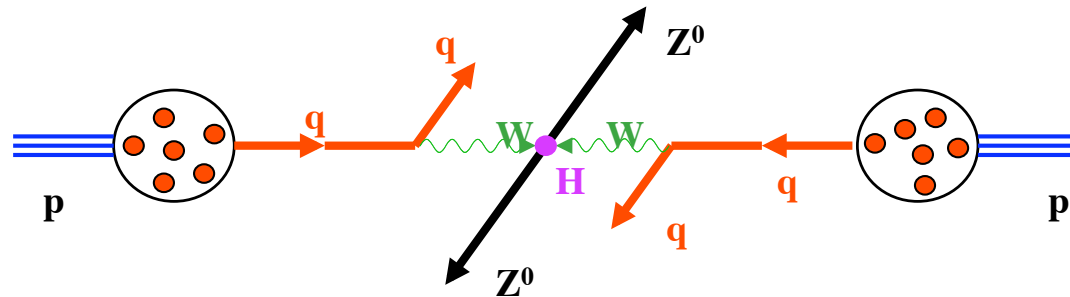
Event size:

~ 1 Mbyte

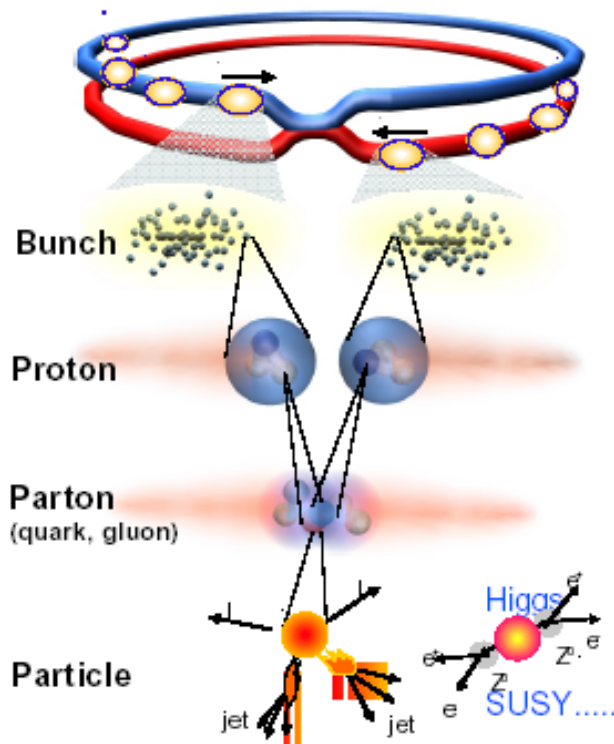
Processing Power:

\sim Multi-TFlop

LHC: a very hostile environment for DAQ (high event rate, high multiplicity, high radiation flux)



Collisions at LHC



Proton-Proton 2835 bunch/beam
 Protons/bunch 10^{11}
 Beam energy 7 TeV (7×10^{12} eV)
 Luminosity $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$

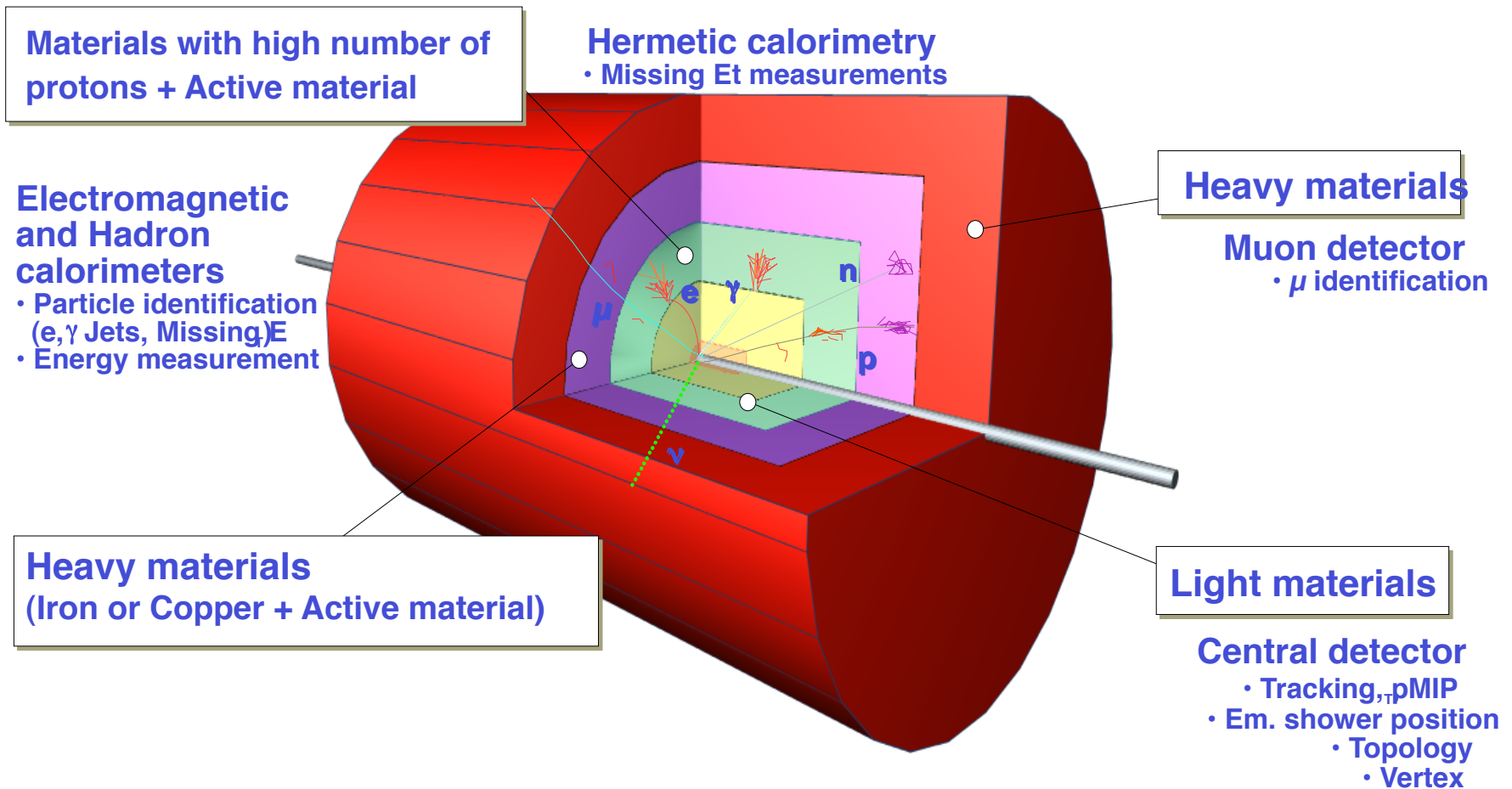
Crossing rate 40 MHz

Collisions rate $\approx 10^7 - 10^9$ Hz

New physics rate $\approx .00001$ Hz

Event selection:
 1 in 10,000,000,000,000

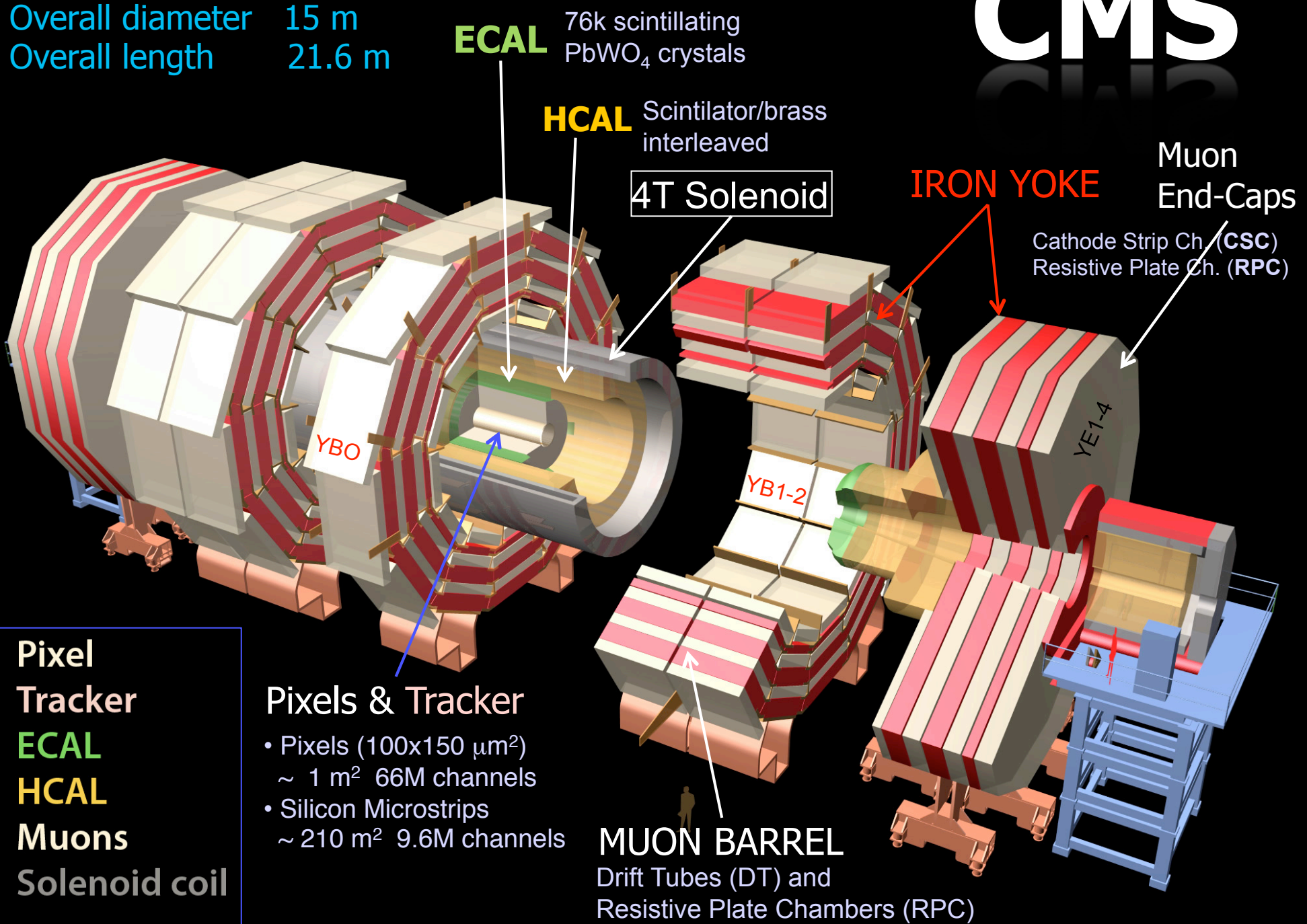
Detectors at LHC



Each layer identifies and enables the measurement of the momentum or energy of the particles produced in a collision

CMS

Total weight 12500 t
Overall diameter 15 m
Overall length 21.6 m



ECAL 76k scintillating PbWO₄ crystals

HCAL Scintillator/brass interleaved

4T Solenoid

IRON YOKE

Muon End-Caps

Cathode Strip Ch. (CSC)
Resistive Plate Ch. (RPC)

YBO

YB1-2

YE1-4

Pixel Tracker
ECAL
HCAL
Muons
Solenoid coil

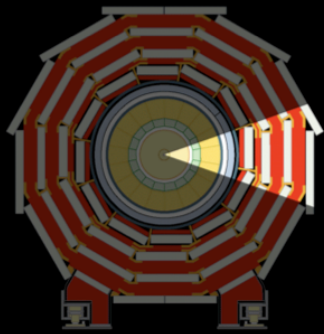
Pixels & Tracker

- Pixels (100x150 μm²)
~ 1 m² 66M channels
- Silicon Microstrips
~ 210 m² 9.6M channels

MUON BARREL
Drift Tubes (DT) and
Resistive Plate Chambers (RPC)

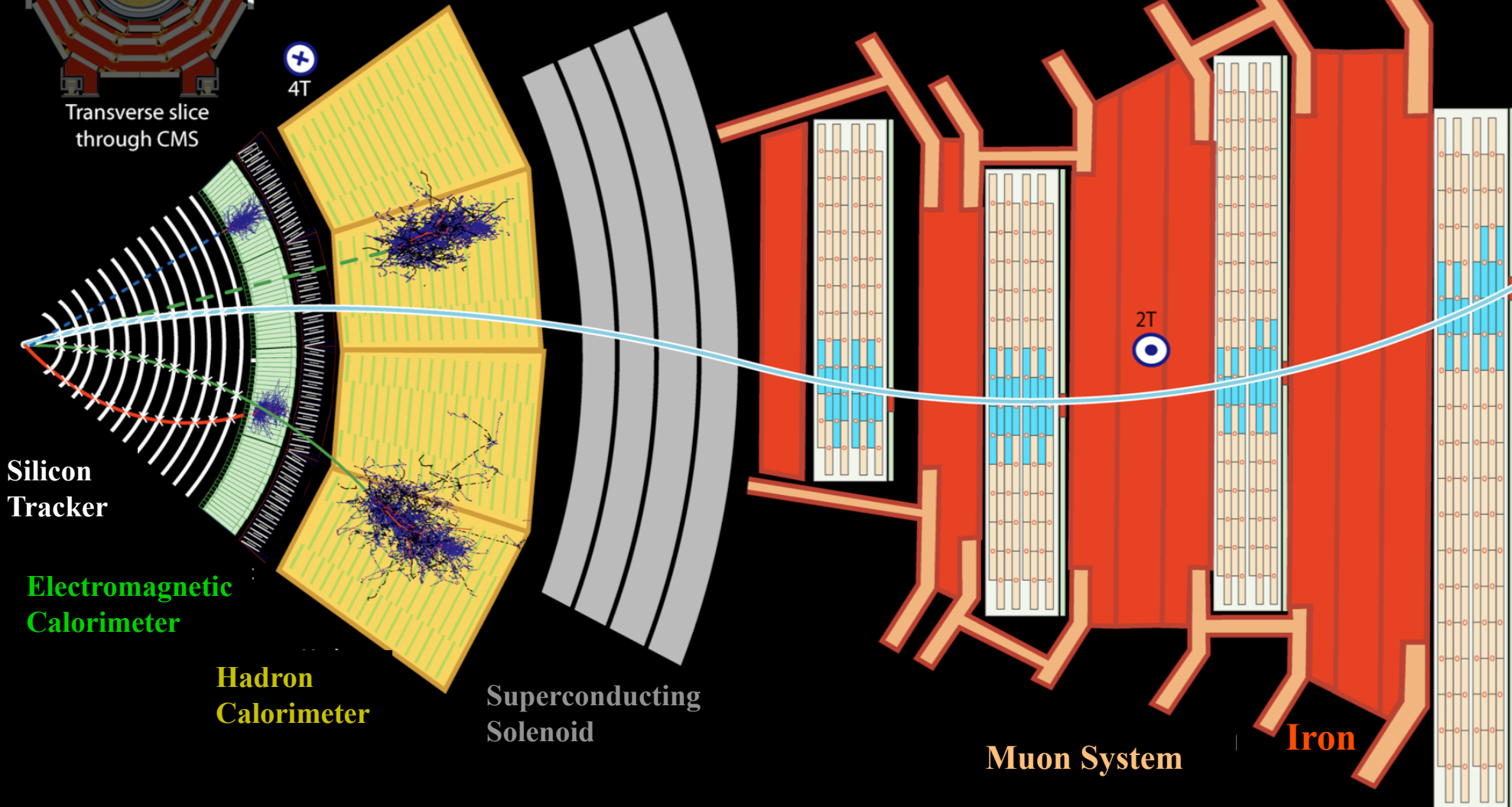
Transverse slice of CMS

- Key:
- Muon
 - Electron
 - Charged Hadron (e.g. Pion)
 - - - Neutral Hadron (e.g. Neutron)
 - ⋯ Photon



Transverse slice through CMS

4T



Silicon Tracker

Electromagnetic Calorimeter

Hadron Calorimeter

Superconducting Solenoid

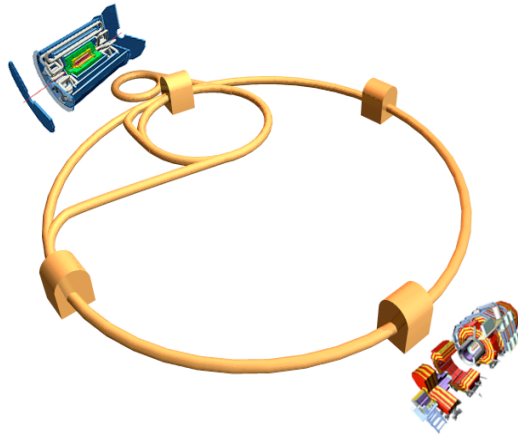
Muon System

Iron

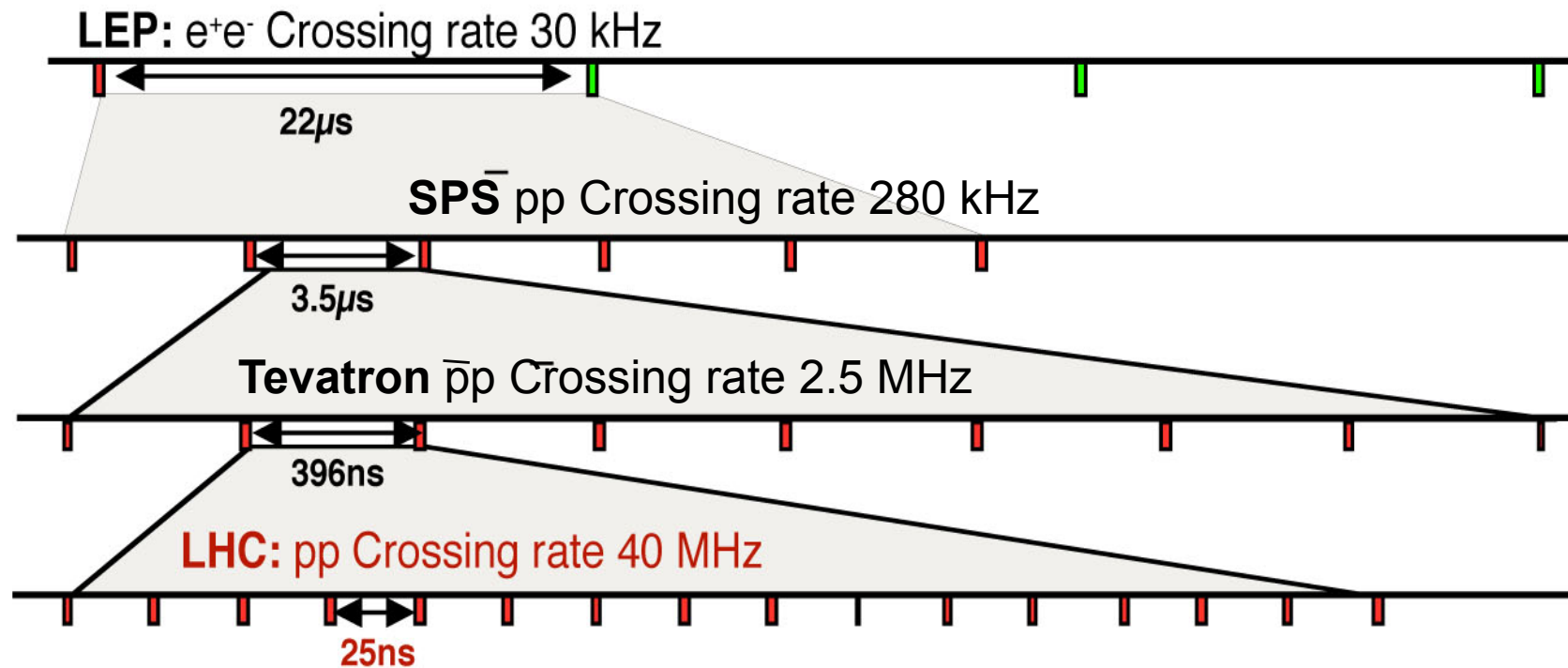




Bunch Crossing Times: LEP, Tevatron & LHC



- LHC has ~3600 bunches (2835 filled with protons)
- And same length as LEP (27 km)
- Distance between bunches: $27\text{km} / 3600 = 7.5\text{m}$
- Distance between bunches in time: $7.5\text{m} / c = \mathbf{25\text{ns}}$



pp cross-sections and minimum bias

of interactions/crossing:

Interactions/s:

$$\text{Lum} = 10^{34} \text{ cm}^{-2}\text{s}^{-1} = 10^7 \text{ mb}^{-1}\text{Hz}$$

$$\sigma_{\text{inel}}(\text{pp}) = 80 \text{ mb}$$

$$\text{Interaction Rate, } R = 8 \times 10^8 \text{ Hz}$$

Events/beam crossing:

$$\Delta t = 25 \text{ ns} = 2.5 \times 10^{-8} \text{ s}$$

$$\text{Interactions/crossing} = 20$$

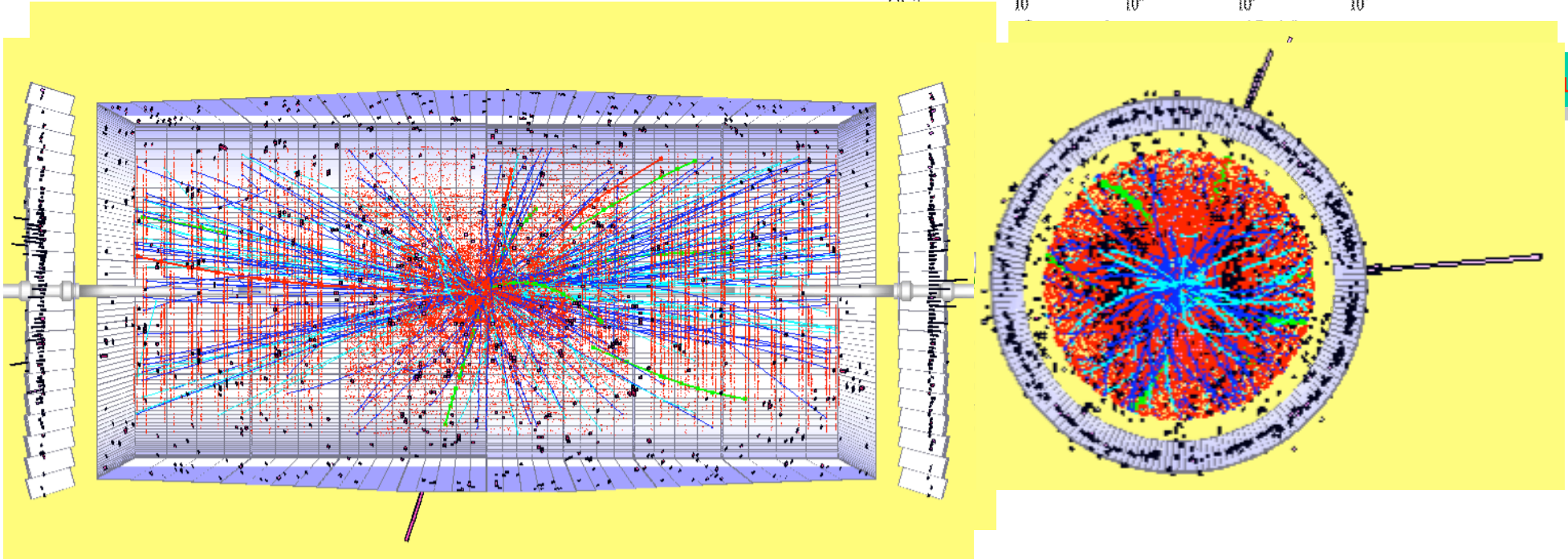
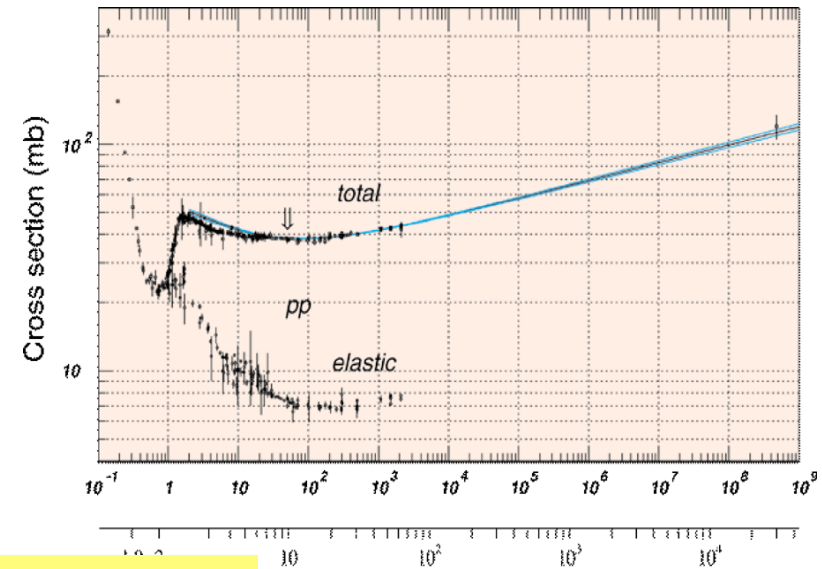
Not all p bunches are full

2835 out of 3564 only

Interactions/"active" crossing =

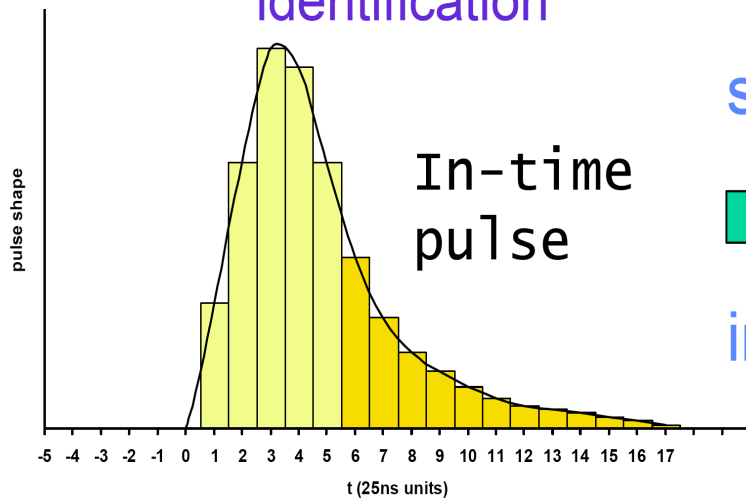
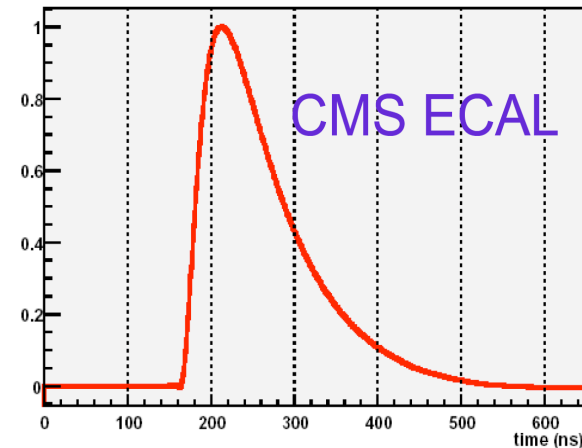
$$= 20 \times 3564 / 2835 = 25$$

$$\sigma_{\text{inel}}(\text{pp}) \approx 80 \text{ mb} @ 14 \text{ TeV}$$

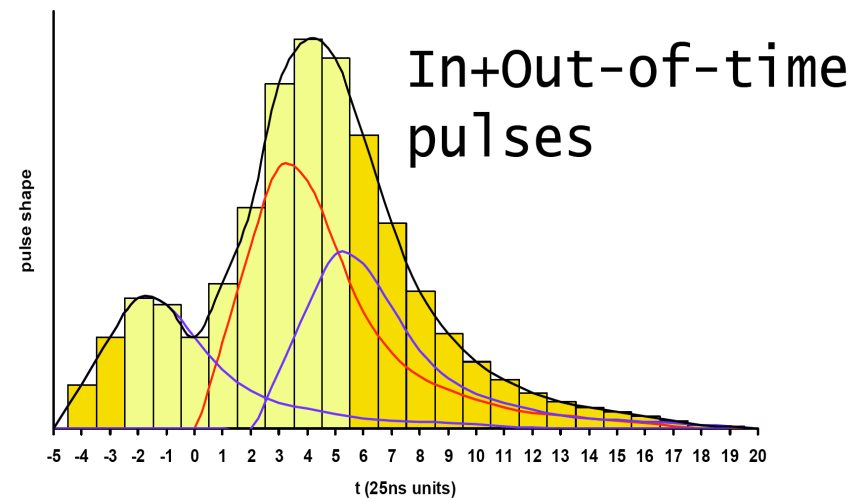



Pile-up

- “In-time” pile-up: particles from the same crossing but from a different pp interaction
- Long detector response/pulse shapes:
 - ◆ “Out-of-time” pile-up: left-over signals from interactions in previous crossings
 - ◆ Need “bunch-crossing identification”



super-
impose

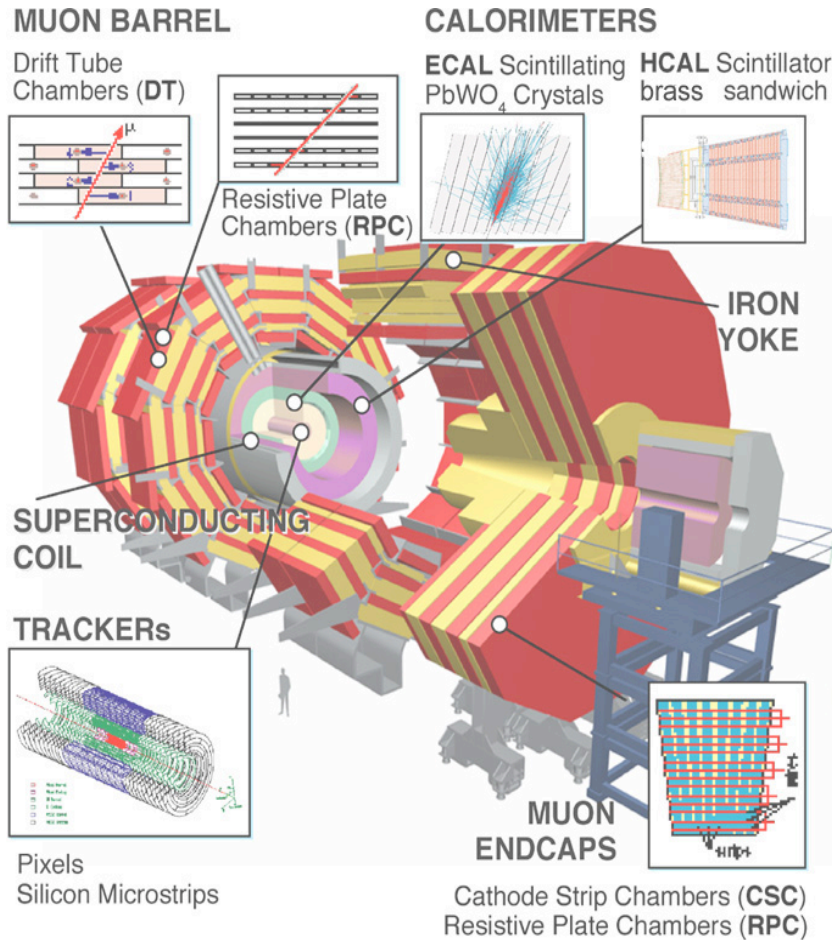




CMS design parameters and DAQ requirements



Detectors



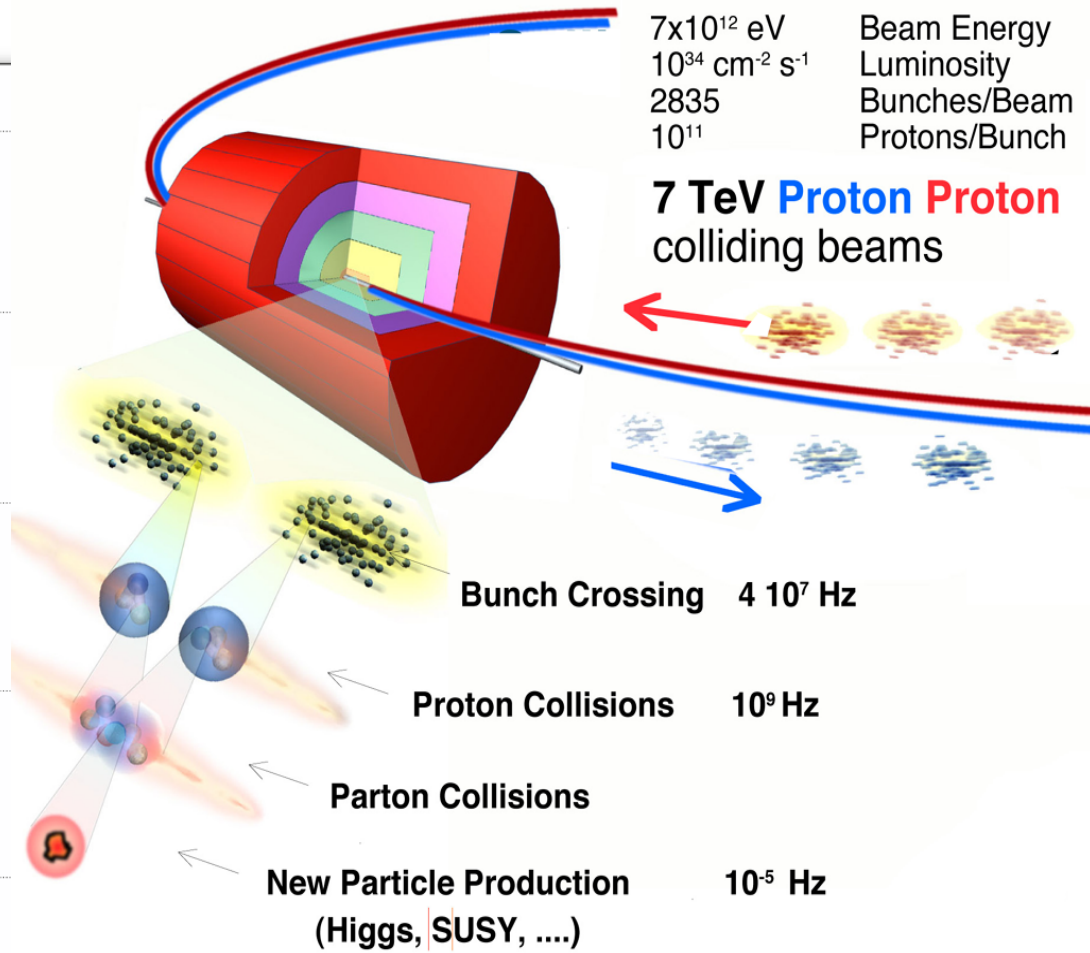
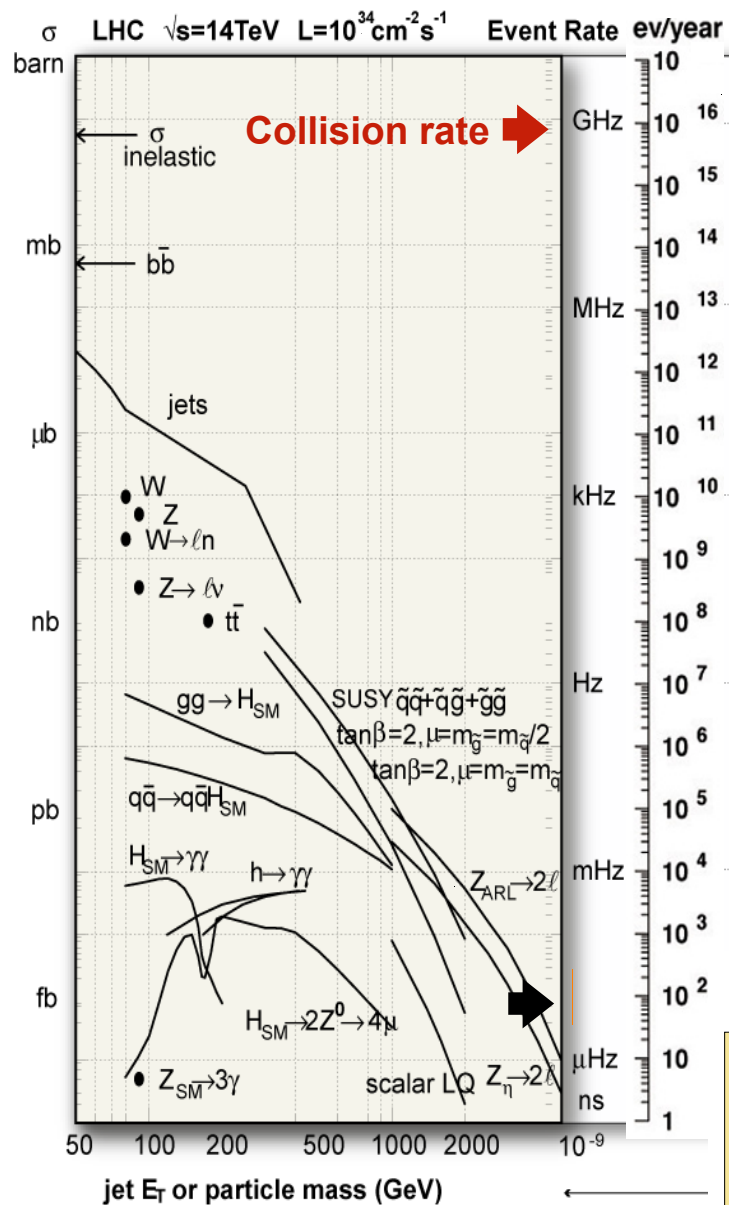
Detector	Channels	Control	Ev. Data
Pixel	60000000	1 GB	50 (kB)
Tracker	10000000	1 GB	650
Preshower	145000	10 MB	50
ECAL	85000	10 MB	100
HCAL	14000	100 kB	50
Muon DT	200000	10 MB	10
Muon RPC	200000	10 MB	5
Muon CSC	400000	10 MB	90
Trigger		1 GB	16

Event size 1 Mbyte
Max LV1 Trigger 100 kHz
Online rejection 99.999%
System dead time ~ %

Total weight : 12,500 t
 Overall diameter : 15 m

Overall length : 21.6 m
 Magnetic field : 4 Tesla

Crossing and Event Rates



Collision Rate: $\sim 10^9$ Hz
Event Selection: $\sim 1/10^{13}$

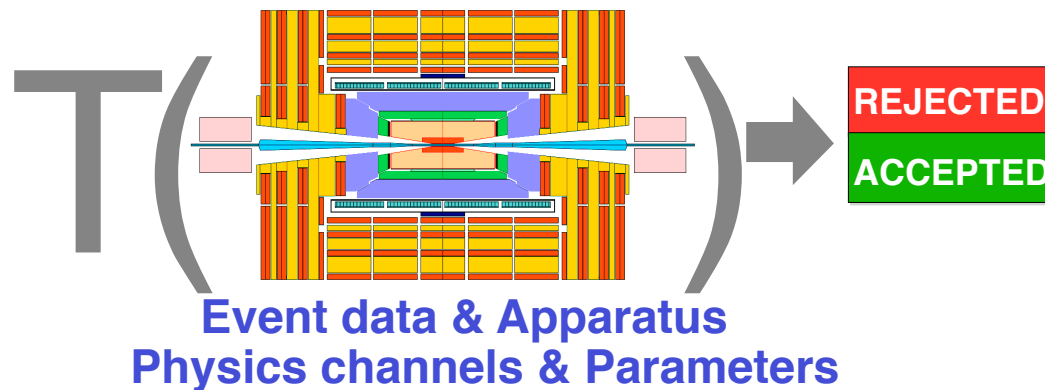
Event selection: The trigger system

Mandate:

"Look at all bunch crossings, select most interesting ones, collect all detector information and store it for off-line analysis"

P.S. For a reasonable amount of CHF

The trigger is a function of :



Since the detector data are not all promptly available and the function is highly complex, $T(\dots)$ is evaluated by successive approximations called :

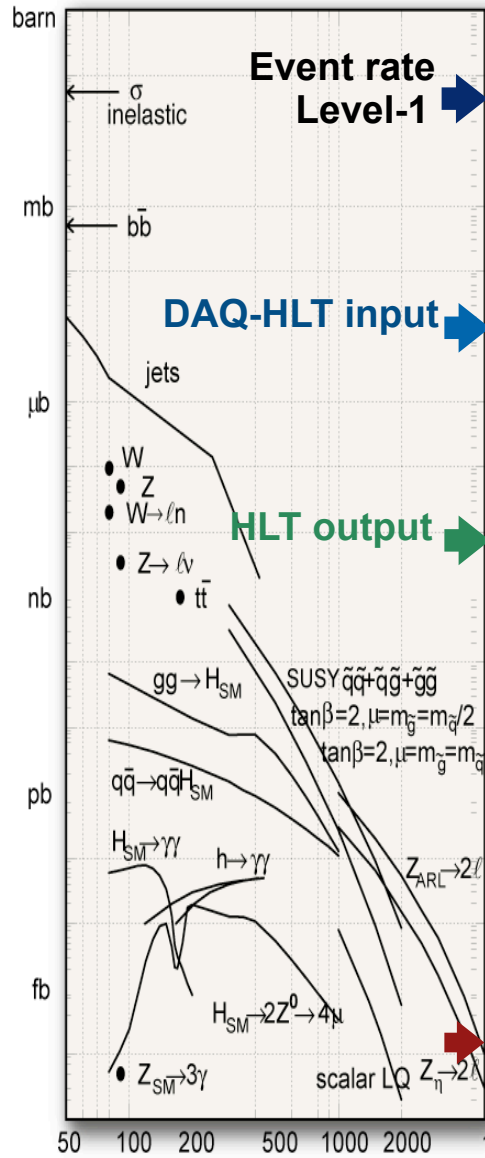
TRIGGER LEVELS
(possibly with zero dead time)



ON/OFF-line data flow and computing model



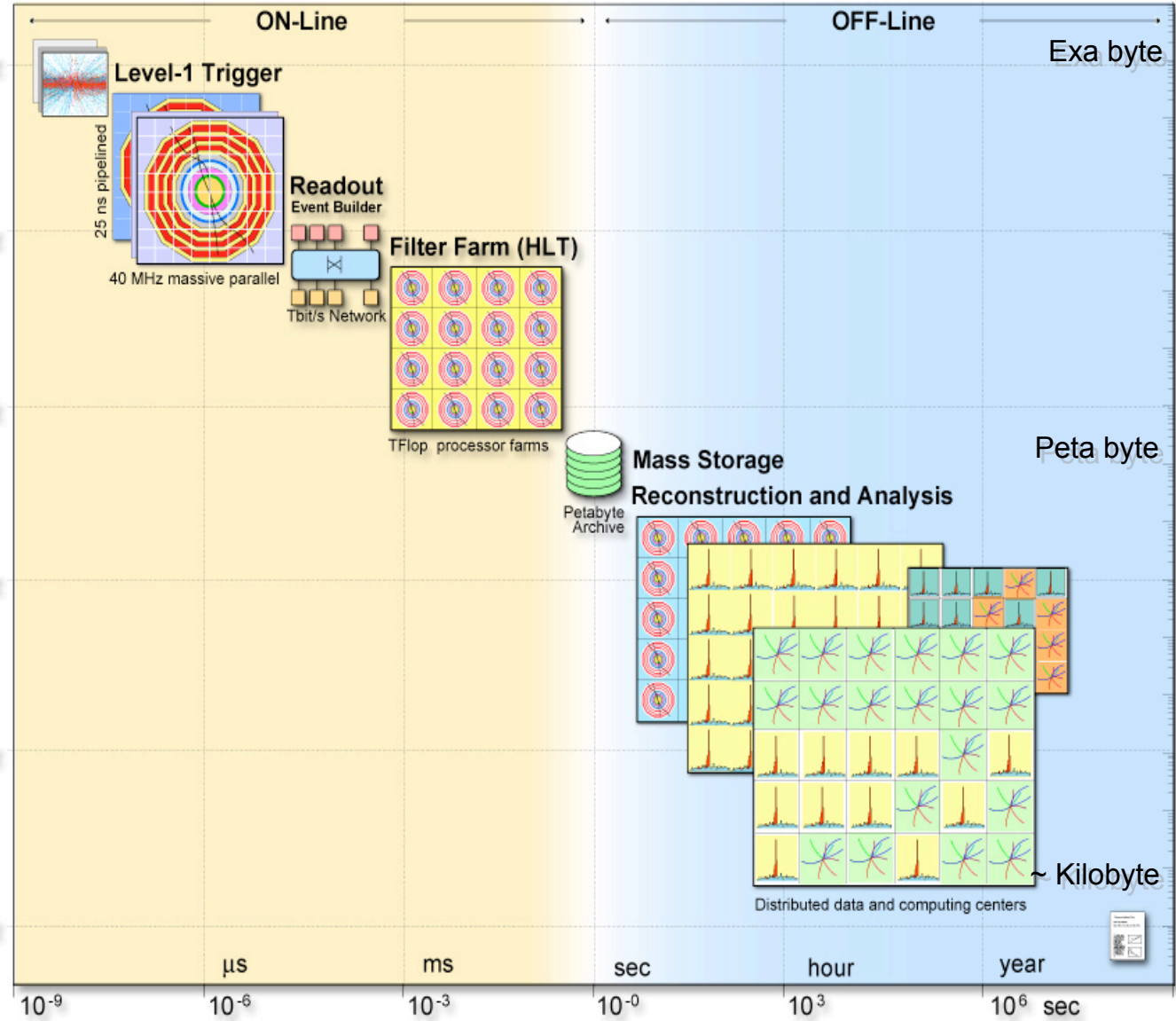
σ LHC $\sqrt{s}=14\text{TeV}$ $L=10^{34}\text{cm}^{-2}\text{s}^{-1}$ Event Rate



Event rate Level-1

DAQ-HLT input

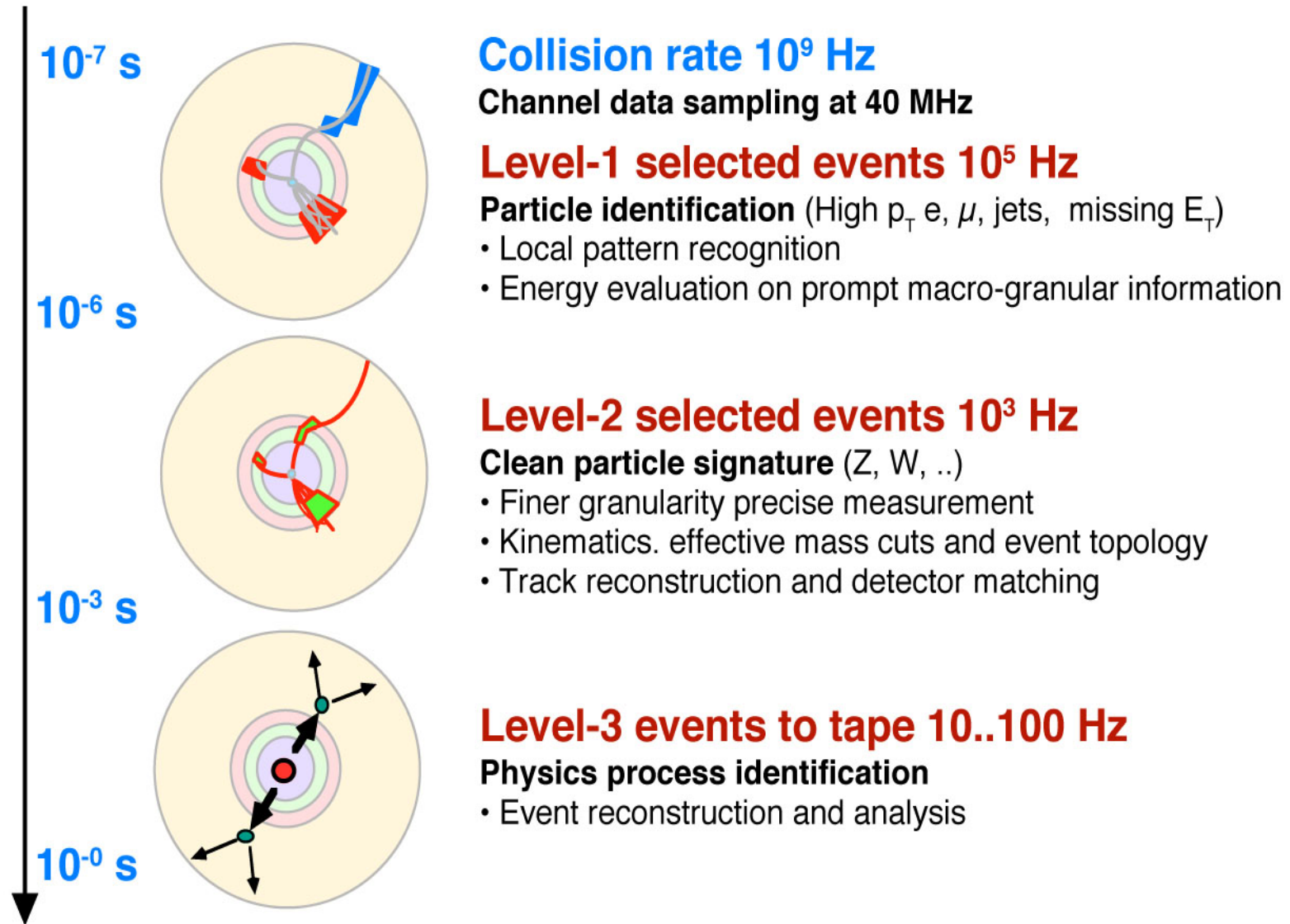
HLT output



jet E_T or particle mass (GeV)



Trigger levels at LHC (the first second)

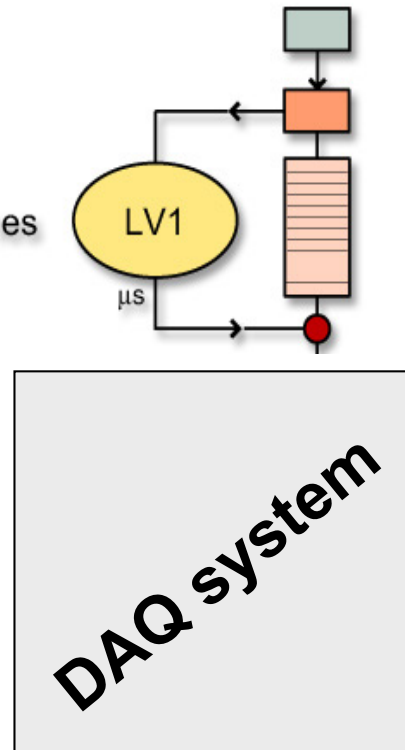


DAQ structure: constraints & requirements

Detectors

Digitizers

Front end pipelines



Collision rate

40 MHz

Detectors

$\sim 10^7$ Channels

3 μ s data pipeline

Level-1 rate

100 kHz

Event size (p-p)

~ 1 Mbyte

Readout bandwidth

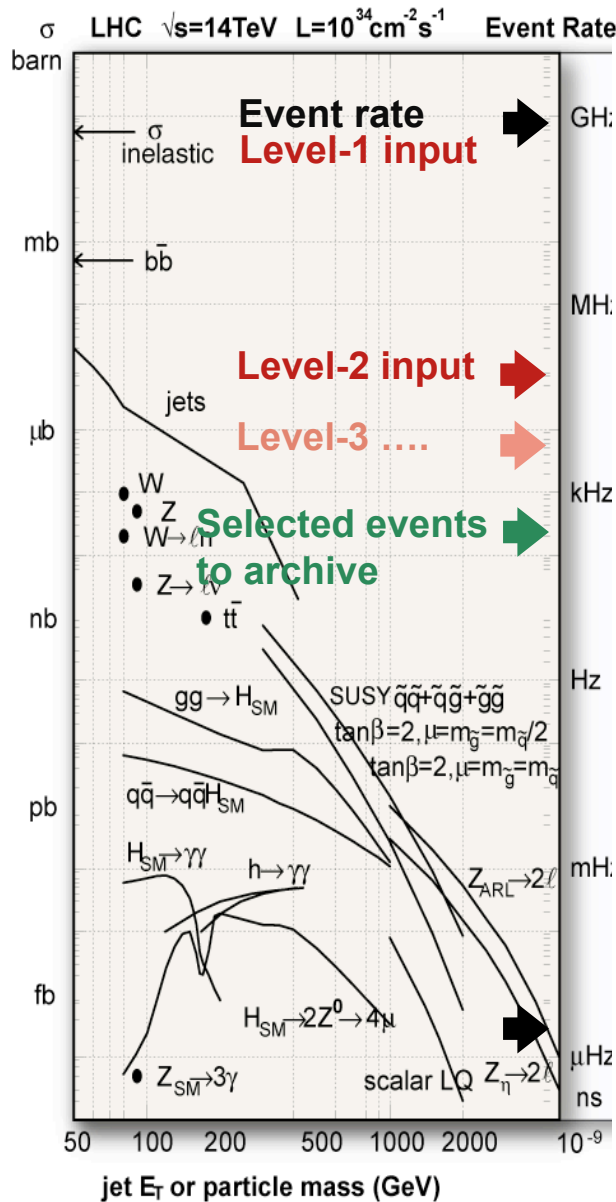
1 Terabit/s

Events to tape

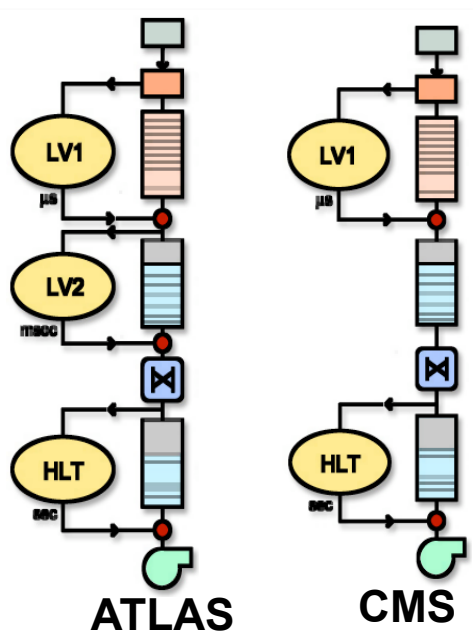
~ 100 Hz



Multi-level trigger DAQ architecture



ON-line
OFF-line



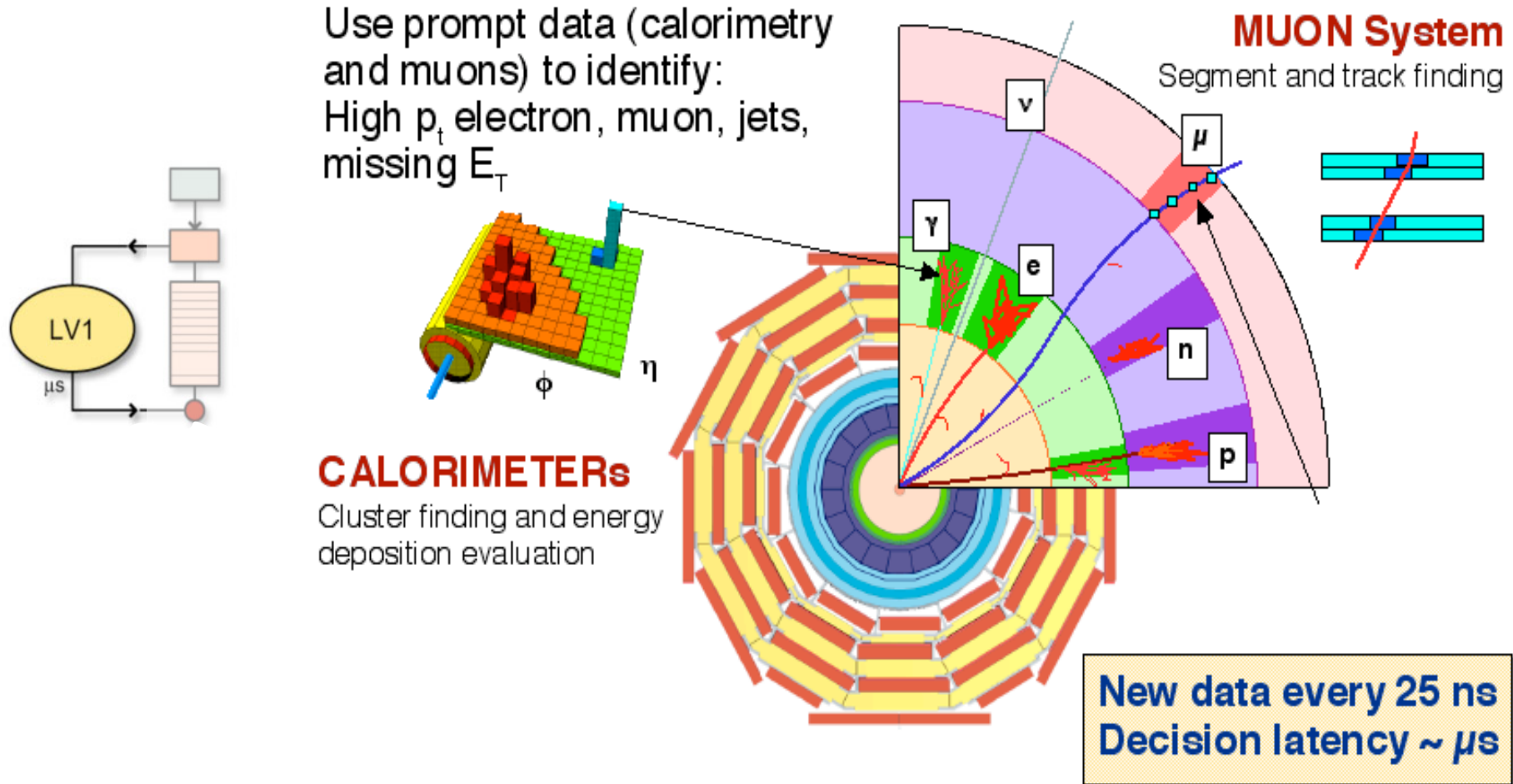
On-line requirements

Collision rate	40 MHz
Event size	1 Mbyte
Level-1 Trigger input	40 MHz
Level-2 Trigger input	100 kHz
Level-3 Trigger input	xx kHz
.....	
Mass storage rate	~100 Hz
Online rejection	99.999%
System dead time	~ %
Participants	Thousands

DAQ design issues

Data network bandwidth (EVB)	~ Tb/s
Computing power (HLT)	~ 10 Tflop
Computing cores	~ 10000
Local storage	~ 300 TB

- Minimize custom design
- Exploit data communication and computing technologies
- DAQ staging by modular design (scaling)



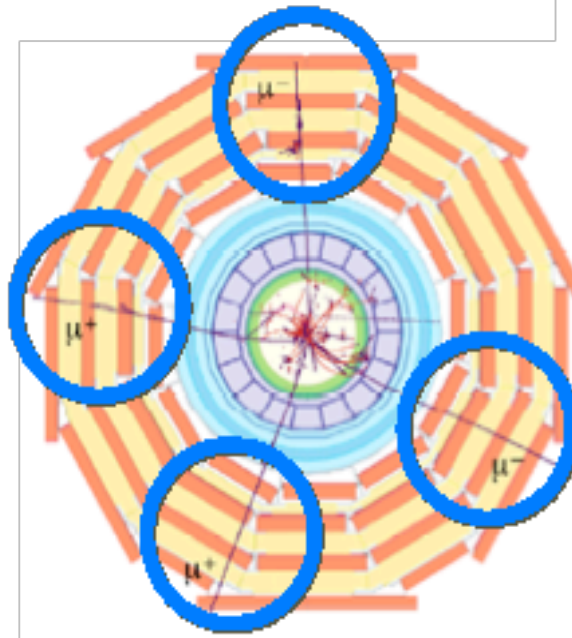
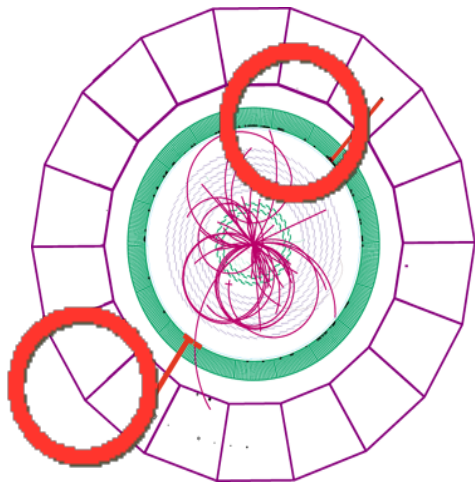
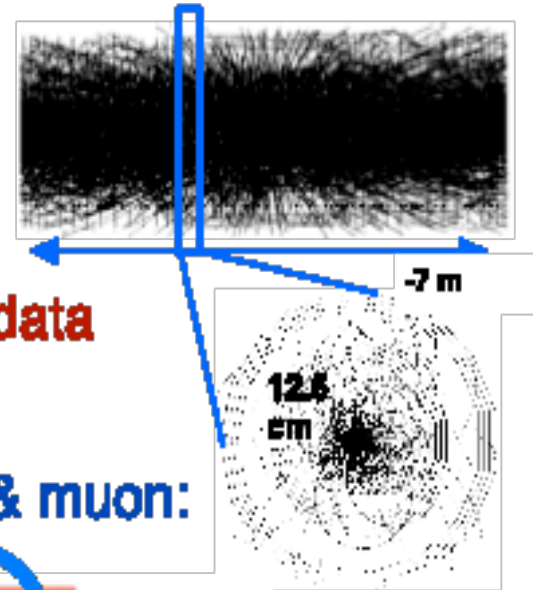
Reduce event rate (to be readout) from 40 MHz to 10^5 Hz

Level-1. Calorimeters and Muons

Compare to Central tracking at $L = 10^{34}$
(50 ns integration, ~1000 tracks)

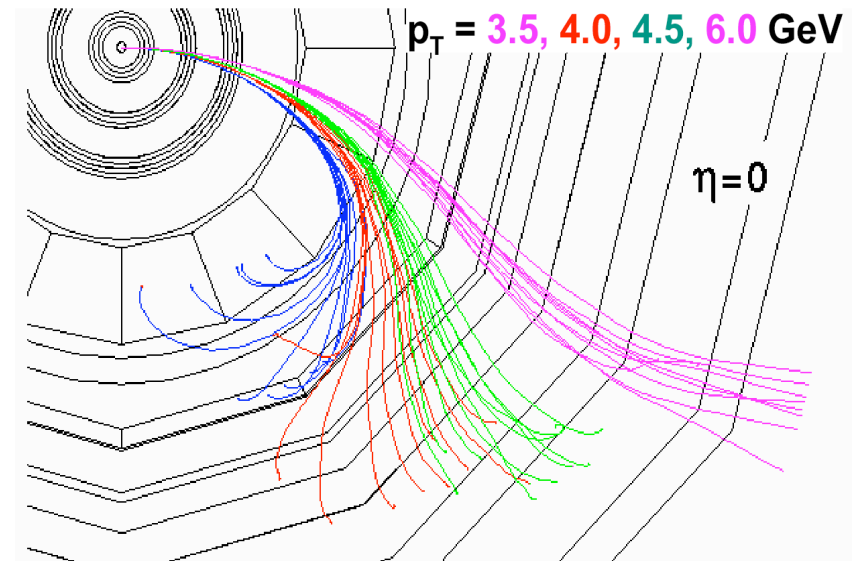
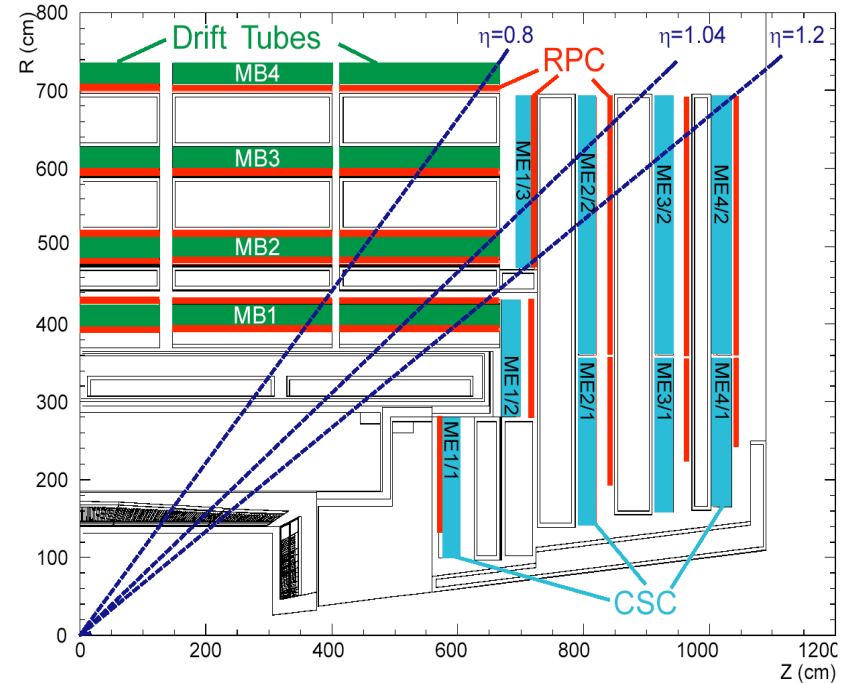
Algorithm Complexity + huge amount of data

Pattern recognition much easier on calo & muon:

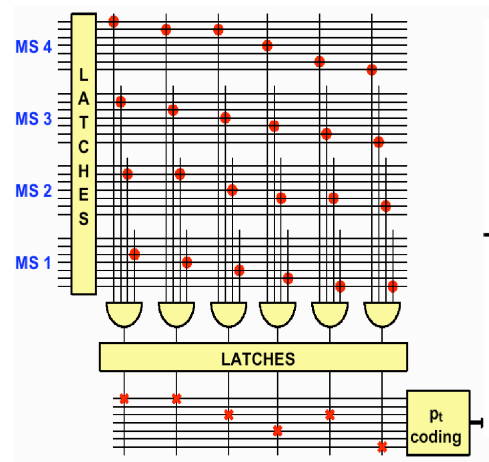
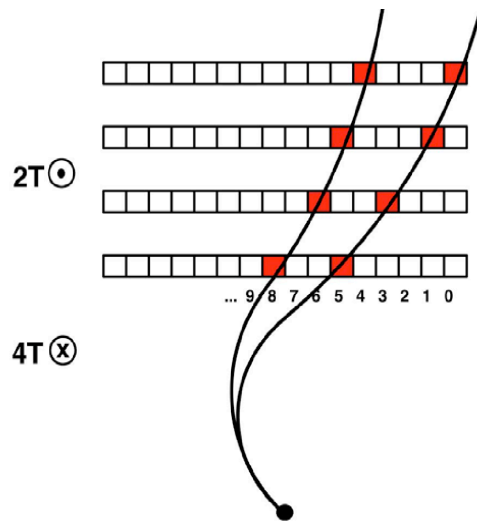


Level-1 Muon: CMS

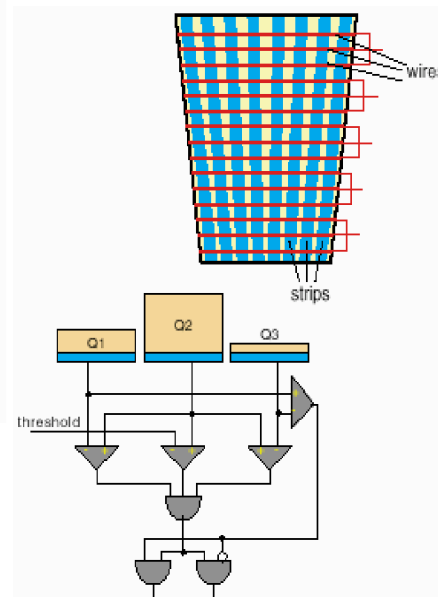
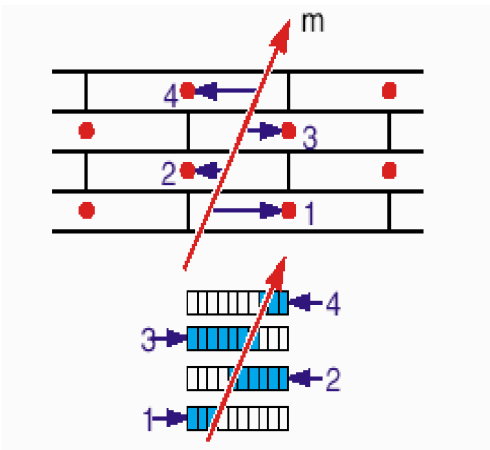
- Level-1 μ -trigger info from:
 - Dedicated trigger detectors:
RPCs (Resistive plate chambers)
 - Excellent time resolution
 - Muon chambers with accurate position resolution
 - Drift Tubes (DT) in barrel
 - Cathode Strip Chambers (CSC) in end-caps
 - **Bending in magnetic field**
 \Rightarrow **determine p_T**



Local Track finding



RPC: pattern recognition using pre-calculated pattern table



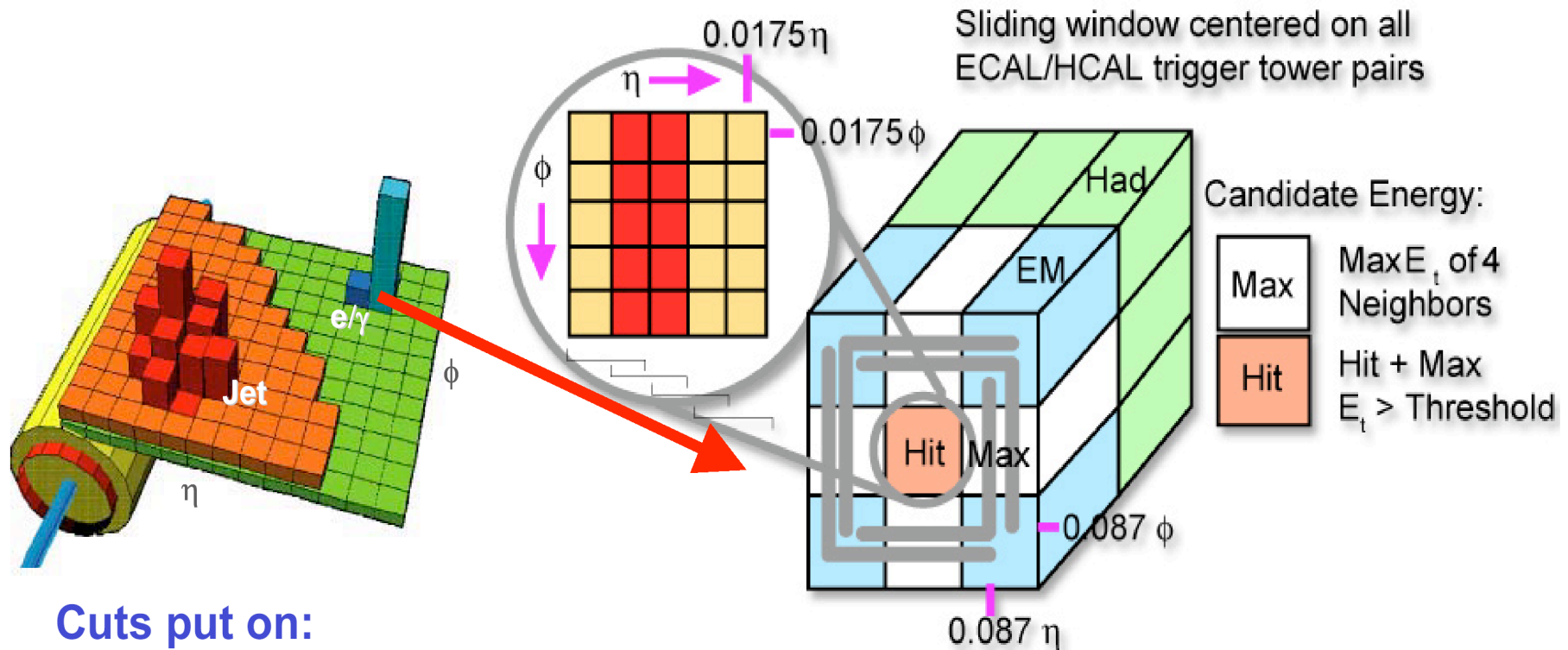
DT: Meantimers form track vectors

Correlation engine combines tracks into segments

CSC: Pattern comparator with half-strip resolution. Hits combined to form track segment

Level-1 Calo: Isolated electron at CMS

- Electromagnetic trigger based on 3×3 trigger towers
 - Each tower is 5×5 crystals in ECAL (barrel; varies in end-cap)
 - Each tower is single readout tower in HCAL



Cuts put on:

- e/h fraction
- Fine shape in ECAL (acts as local isolation)
- Isolation in both ECAL and HCAL sections

Trigger threshold on sum of two towers

CMS Level-1

- Information from calorimeters and muon detectors

- Custom-built electronics for trigger processors (ASICs, FPGAs)

- Synchronous, pipelined

- Processing logic: 25 ns pipelined system
- Must work dead time free
- Latency: $< 3.2 \mu\text{s}$ (128 bx)
- readout + processing: $< 1 \mu\text{s}$
- signal collection + distribution: $\sim 2 \mu\text{s}$

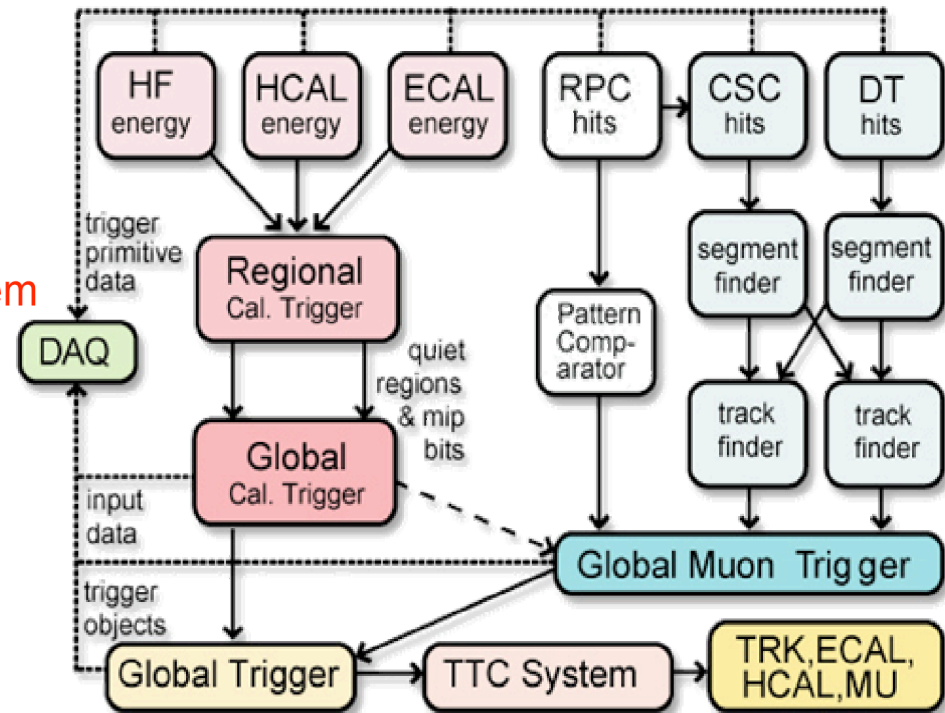
- Max. output rate: 100 kHz

- Organized in 3 subsystems:

- Muon Trigger, Calorimeter Trigger, Global Trigger

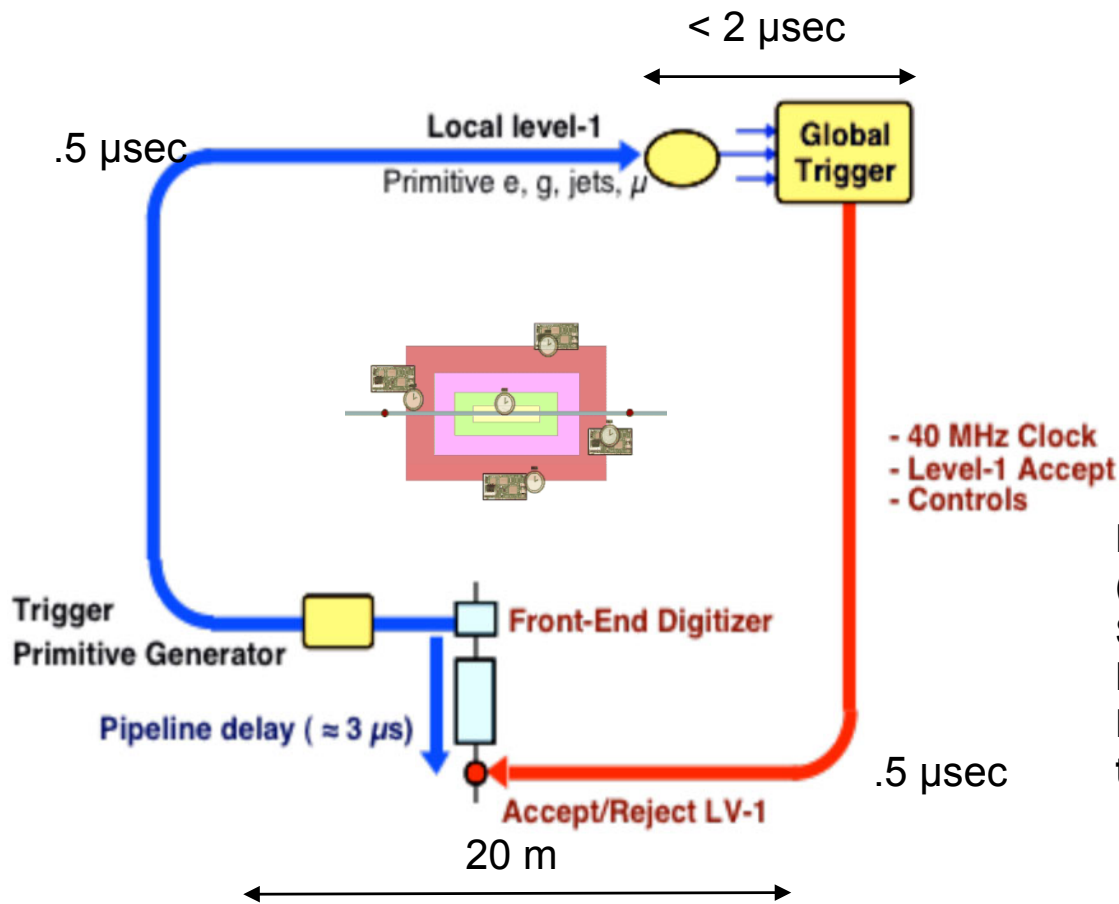
- Backgrounds are huge

- Large rejection factor: 40 MHz ($\times 20$ events/crossing) \rightarrow 100 kHz
- Rates: steep functions of thresholds

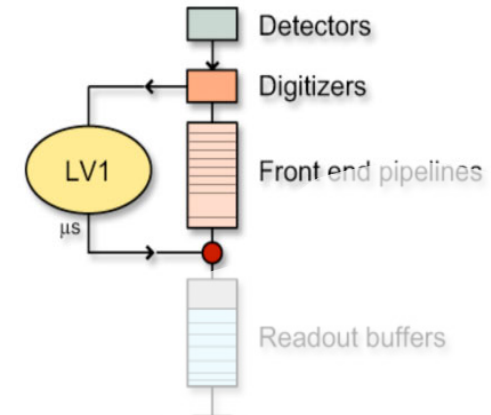




Trigger and data timing loop



Front-end pipeline readout



Front-end time budget

($3.2 \mu\text{s} = 128$ Bunch crossings)

Signals to central logic

18bx 450 ns

Muon/Calo logic

90bx 2250 ns

Back to detectors

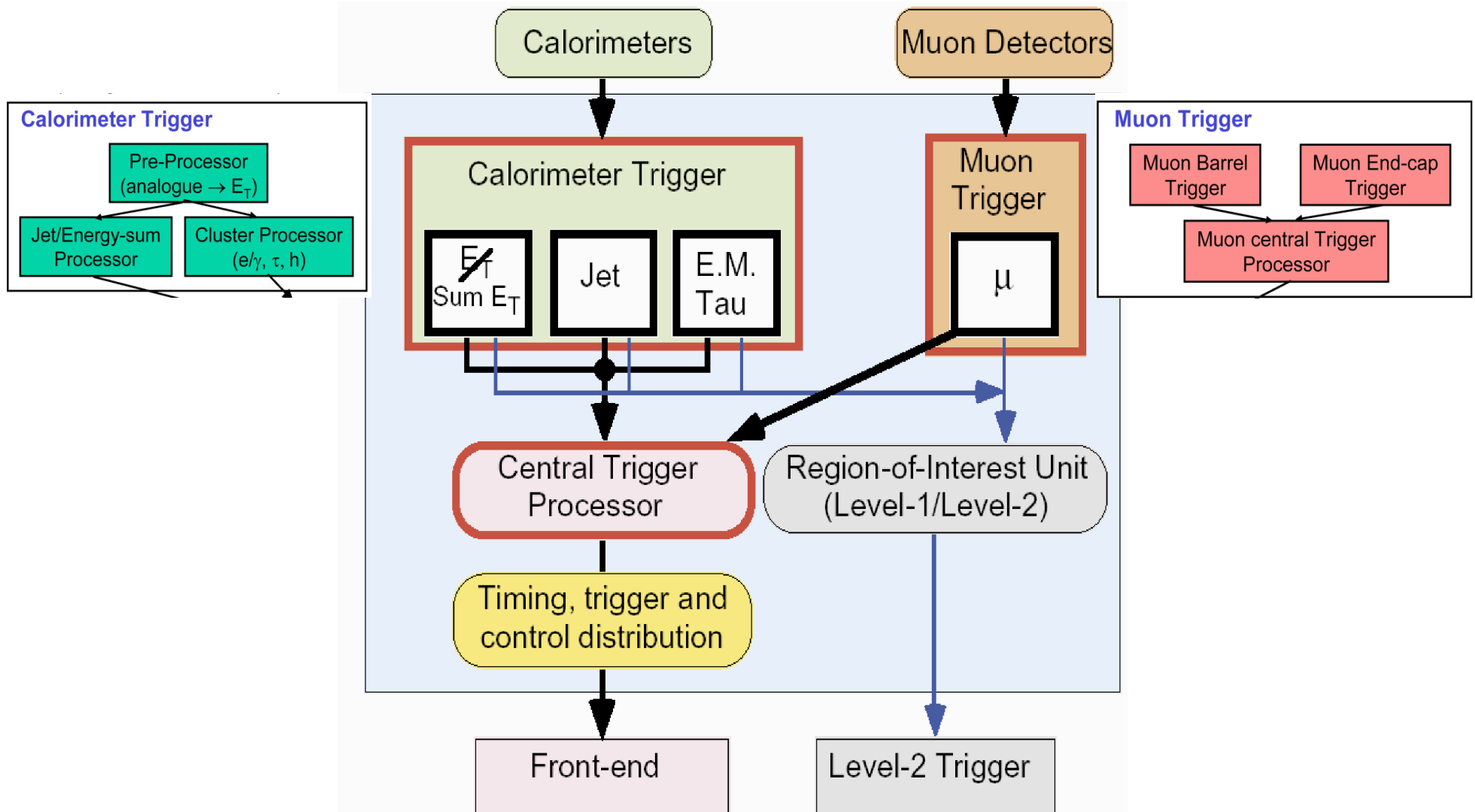
18bx 450 ns

total latency

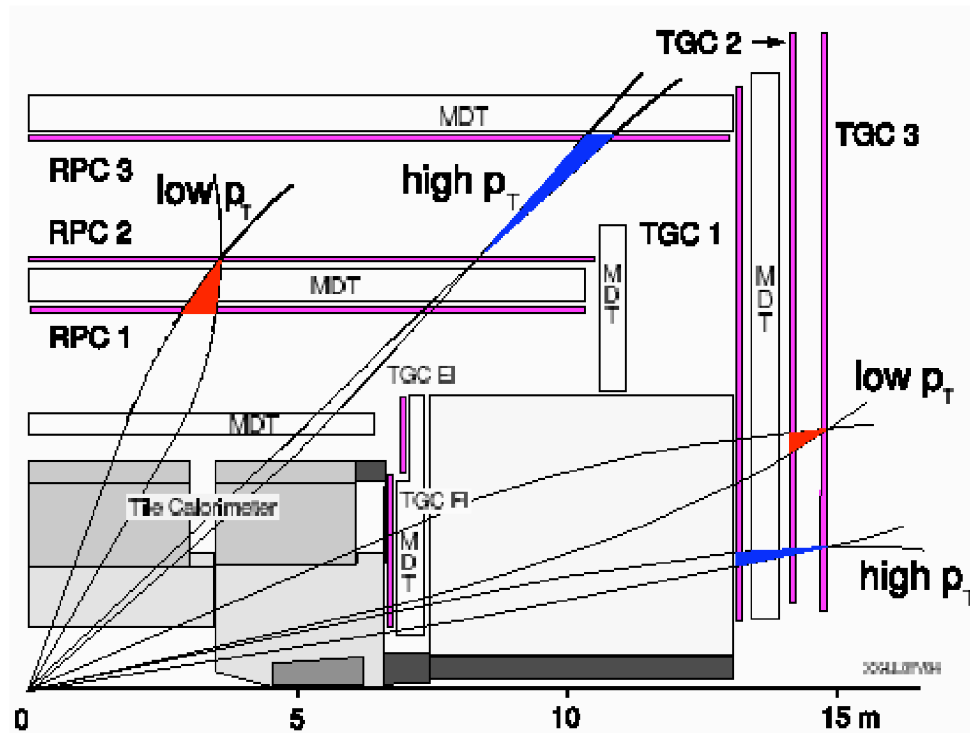
$\leq 128\text{bx}$ $3.2 \mu\text{s}$

40 MHz digitizers and $3.2 \mu\text{s} \times 25\text{ns}$ step pipeline readout buffers
 40 MHz Level-1 trigger (massive parallel pipelined processors)
 High precision ($\sim 100\text{ps}$) timing, trigger and control distribution

ATLAS Level-1



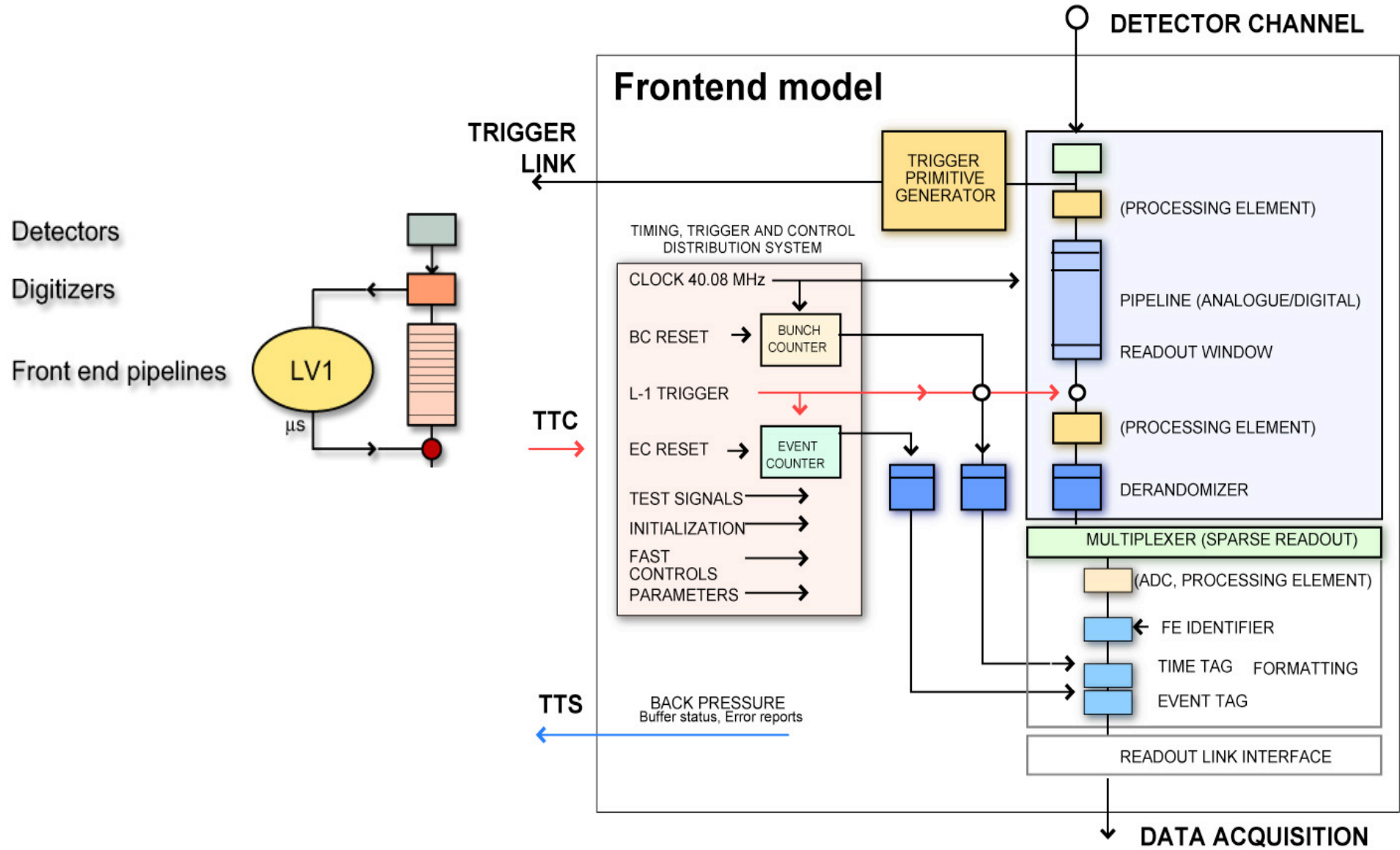
Level 1 Muon: ATLAS



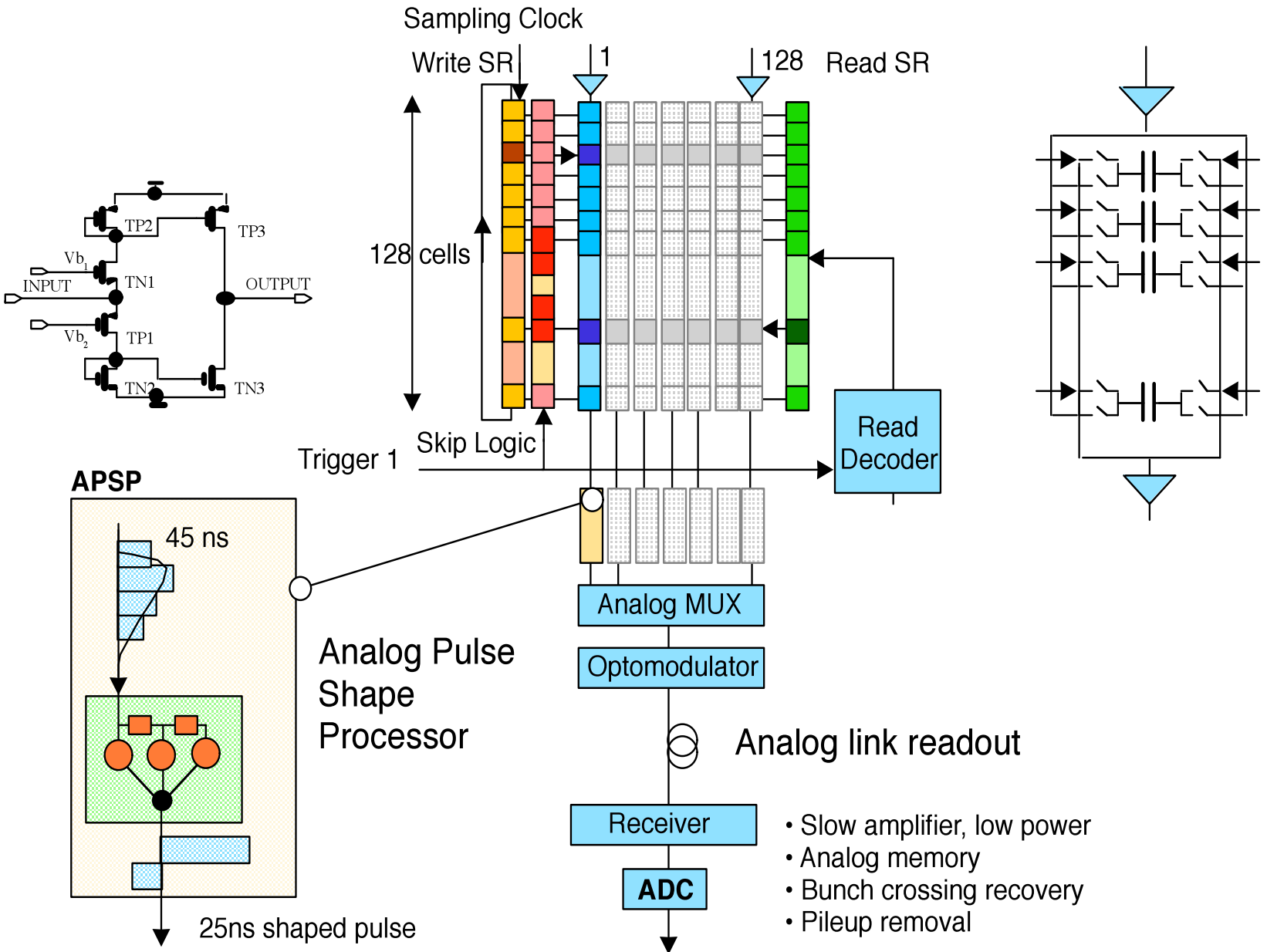
The Level-1 trigger logic is almost fully programmable; this flexibility will allow to optimize carefully the signal trigger efficiency vs. the background rejection.

- RPC in barrel regions
 - 3 stations
 - 430,000 channels
- TGC (Thin Gap Chambers) in end-cap regions
 - 3 stations
 - 800,000 channels
- Coincidence logic (η and ϕ)
- Two p_T threshold ranges
 - **Low p_T (6 – 10 GeV):**
 - Require hits in 3 out of 4 layers in inner two stations
 - **High p_T (8 – 35 GeV):**
 - Require hits in 3 out of 4 layers in inner two stations
 - Require hits in 1 out of 2 layers of the outer station (2 out of 3 in the end-caps)

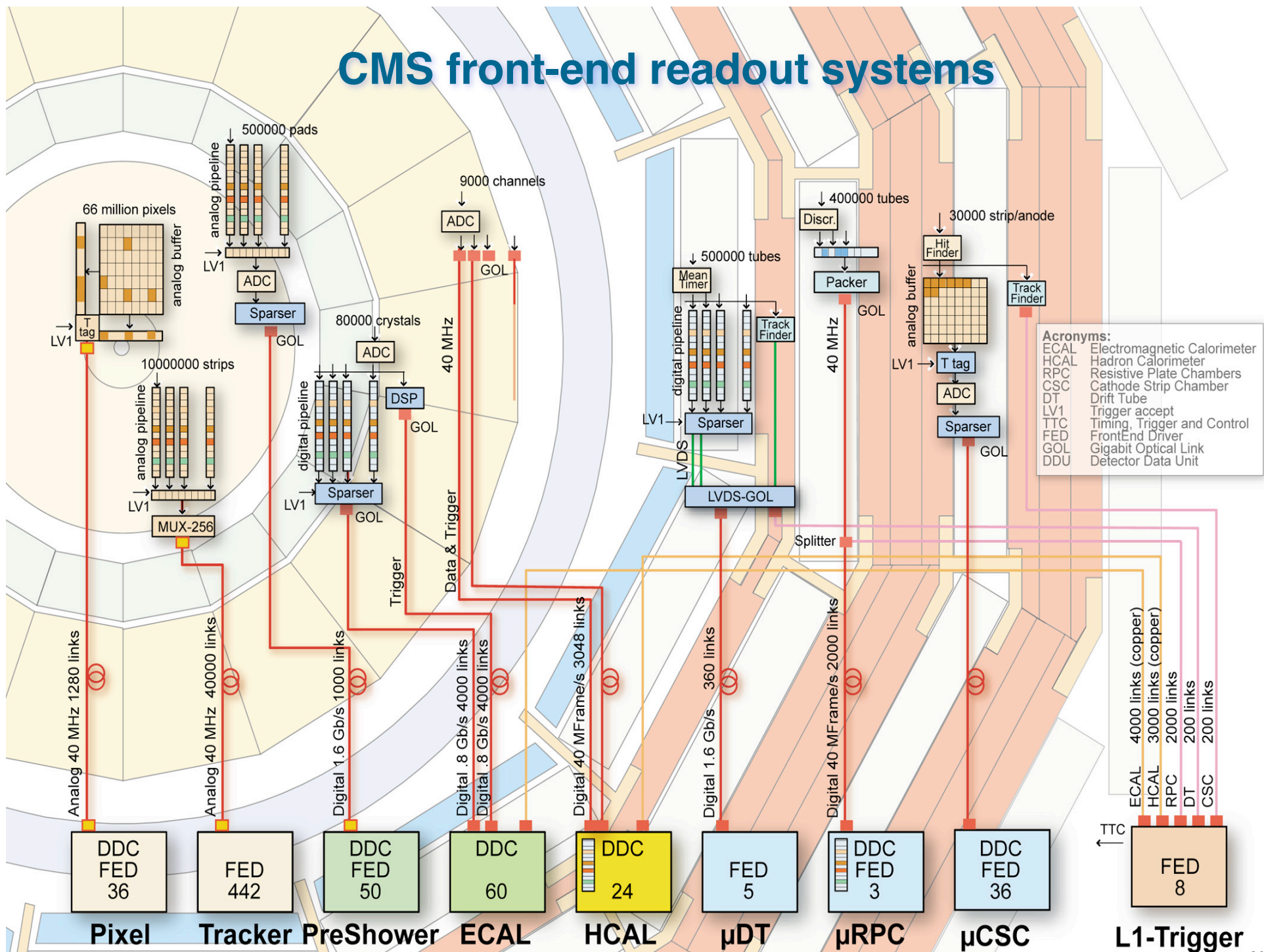
Detector front-end structure



E.g. CMS silicon strip front-end



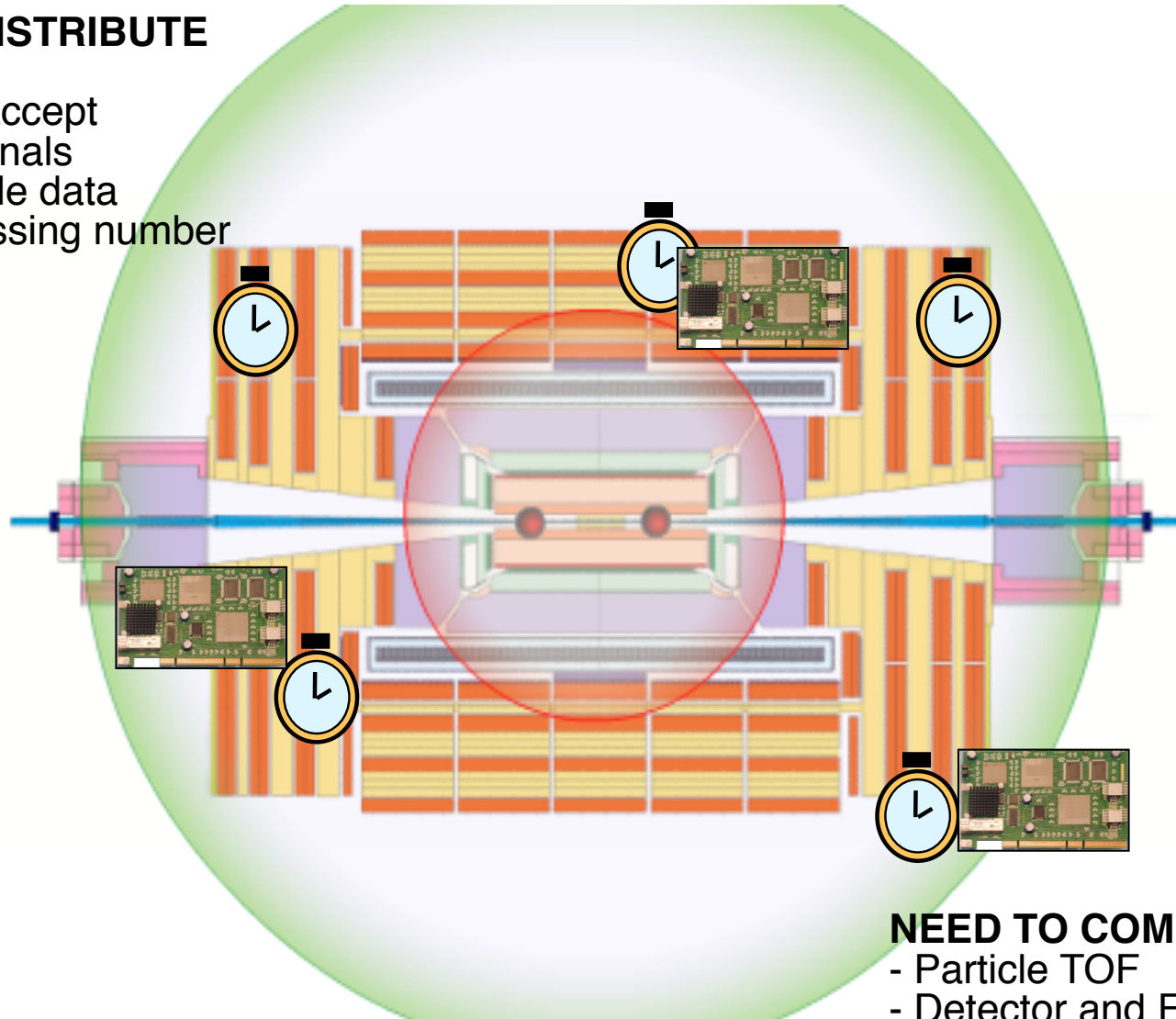
CMS front-end readout systems



Front-end synchronization

NEED TO DISTRIBUTE

- LHC clock
- Trigger-1 accept
- Control signals
- Addressable data
- Bunch crossing number

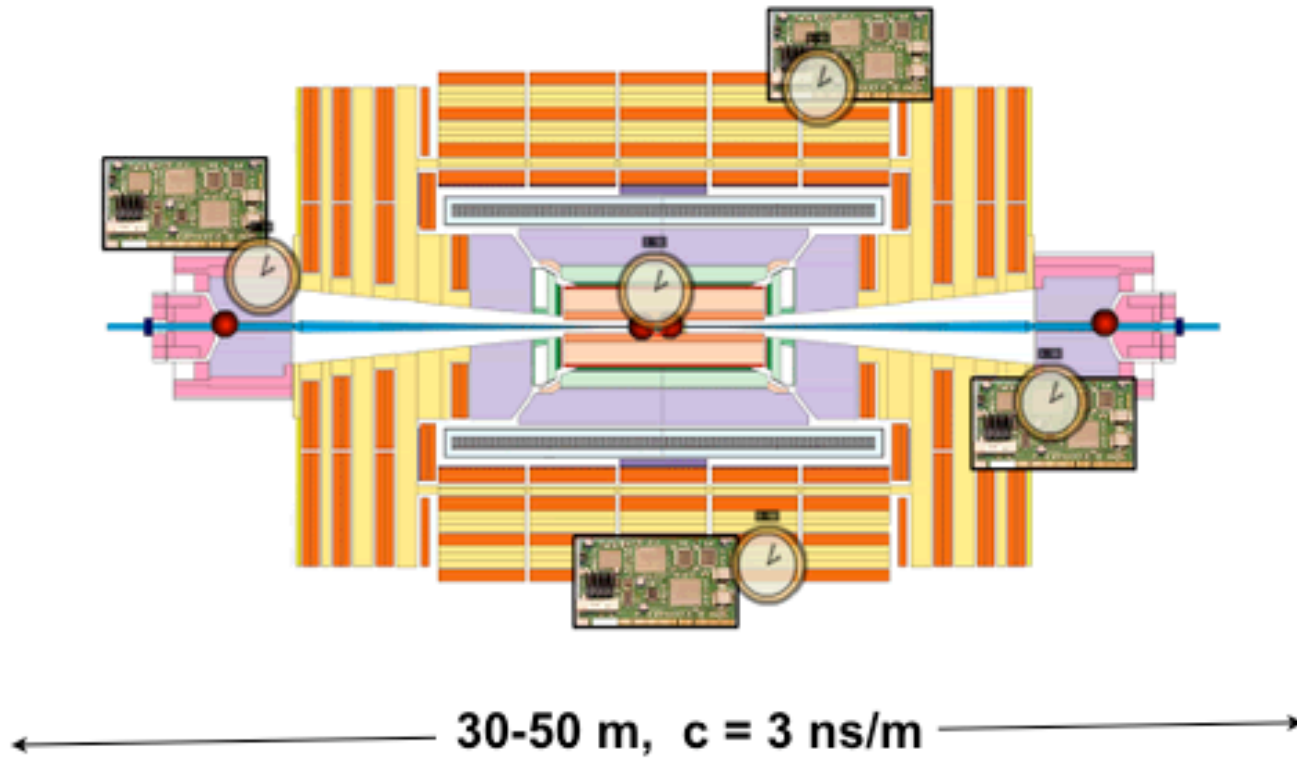


NEED TO COMPENSATE

- Particle TOF
- Detector and Electronics
- Propagation delays (≈ 200 ps)



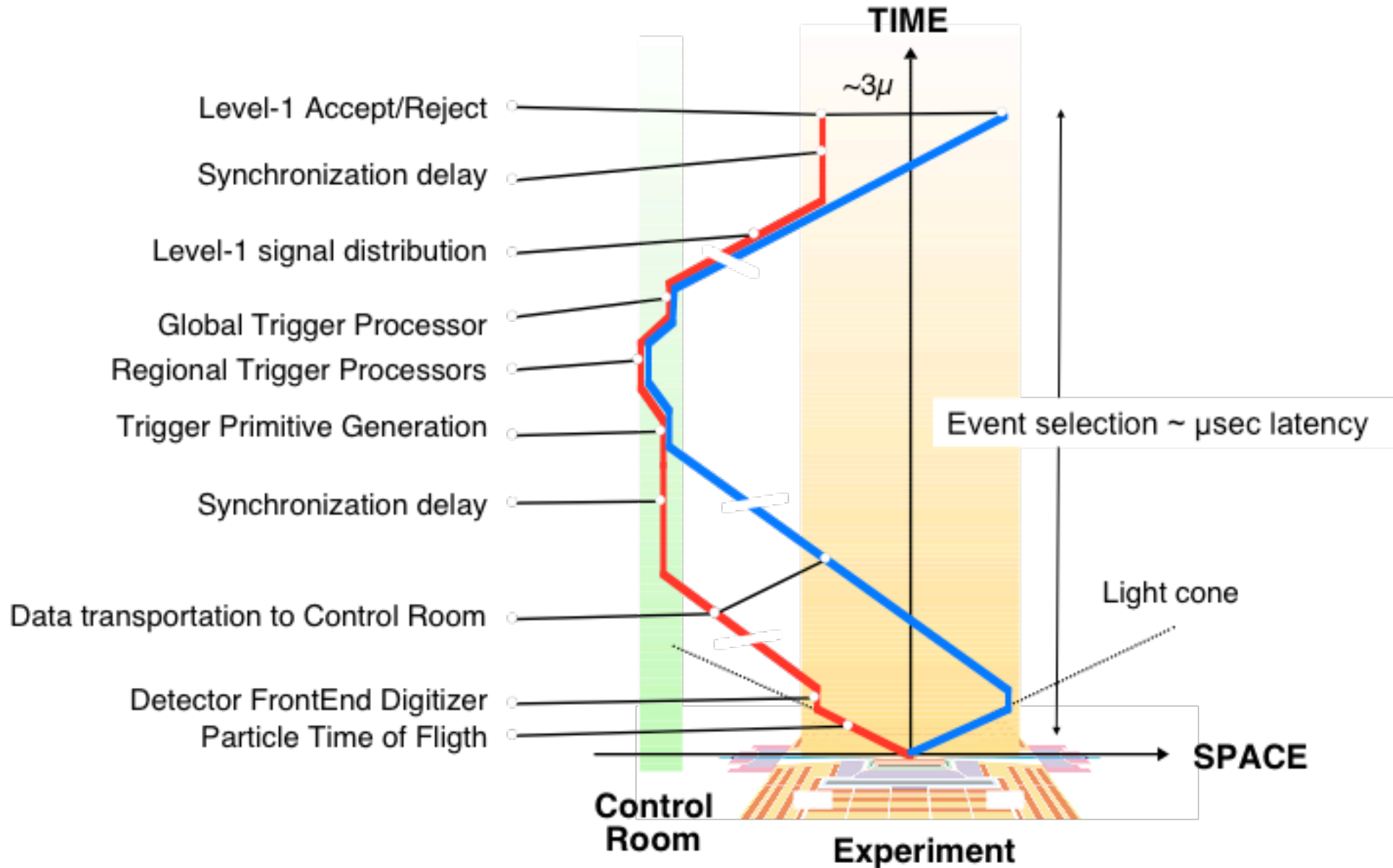
- LHC has ~3600 bunches (2835 filled with protons)
- And same length as LEP (27 km)
- Distance between bunches: $27\text{km} / 3600 = 7.5\text{m}$
- Distance between bunches in time: $b_x = 7.5\text{m} / c = 25\text{ns}$
- Apparatus dimensions 30-70 m \rightarrow 5...7 b_x



Space-time constraint

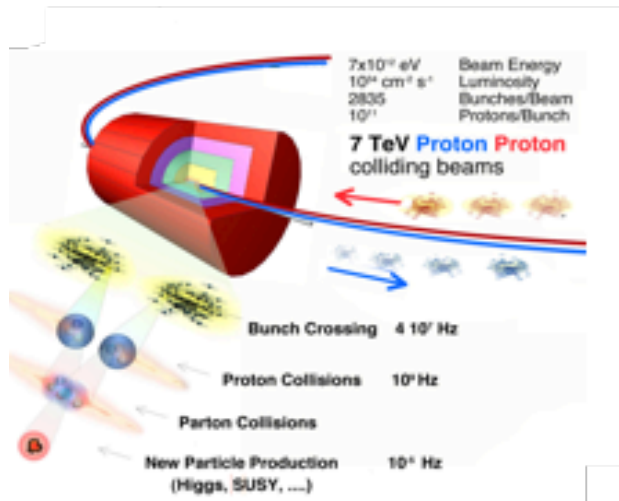
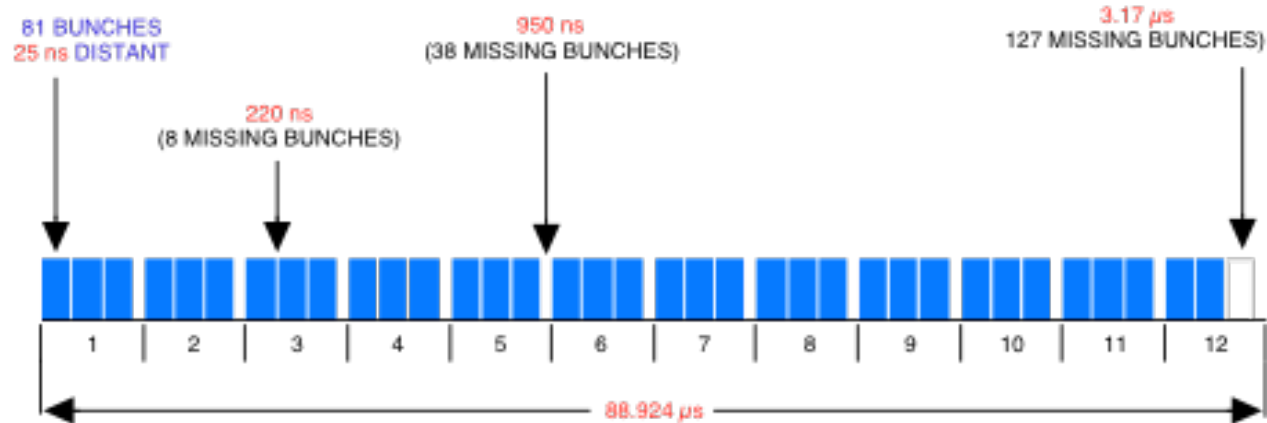


Timing and Trigger and Event kinematics





And things are not always simple



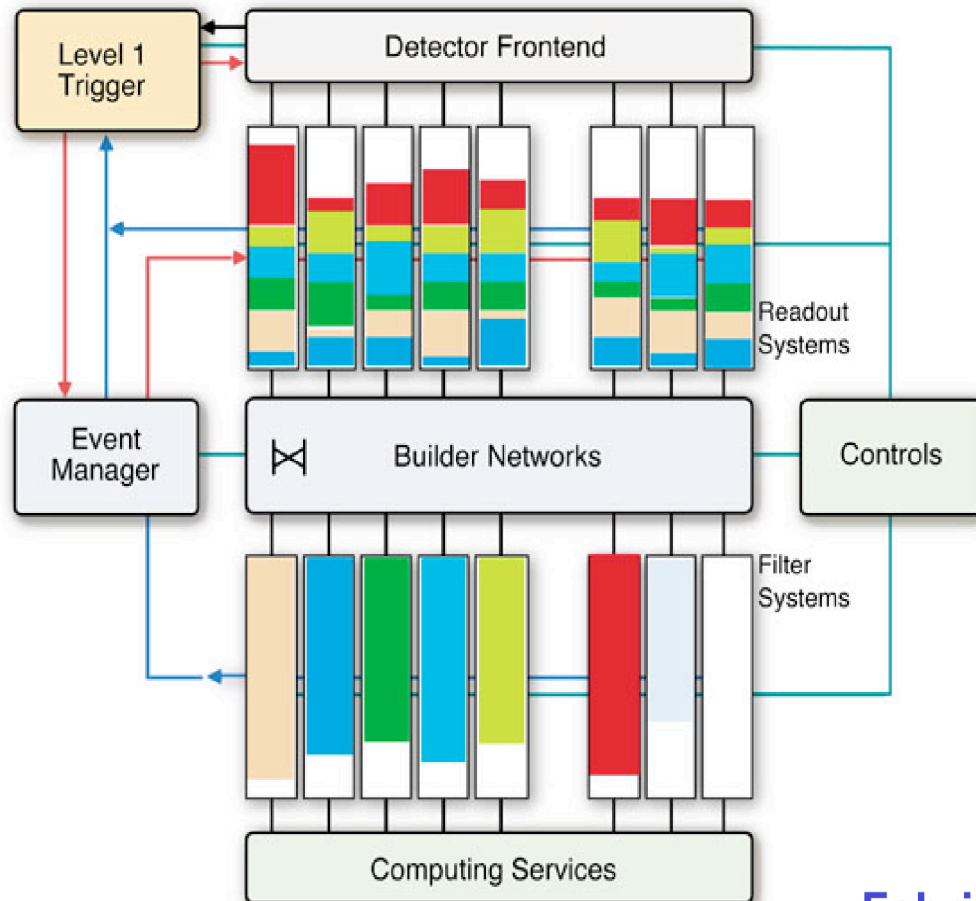
Revolution time	88.924 μs
Revolution frequency	11.246 kHz
RF frequency	400.8 MHz (2 x SPS)
Bunch crossing rate	40.08 MHz
No of bunches/beam	2835
Filling factor	0.795
Bunch train length	81
SPS injection kicker gap	220 ns
LHC injection kicker gap	950 ns
LHC extraction kicker gap	3.17 μs
RMS bunch length	0.075 m
RMS collision length	0.053 m, 177 ps
Interbunch spacing	7.5 m, 25 ns



How to go from 100KHz to 100Hz

- The massive data rate after LVL1 poses problems even for network-based event building — different solutions are being adopted to address this, for example:
 - In CMS, the event building is factorized into a number of slices each of which sees only a fraction of the rate
 - Requires large total network bandwidth (\Rightarrow cost), but avoids the need for a very large single network switch
 - In ATLAS, the **Region-of-Interest (RoI)** mechanism is used with **sequential selection** to access the data only as required – only move data needed for LVL2 processing
 - Reduces by a substantial factor the amount of data that need to be moved from the Readout Systems to the Processors
 - Implies relatively complicated mechanisms to serve the data selectively to the LVL2 trigger processors \Rightarrow more complex software

The Main Challenge: Event Building



Event fragments :
Event data fragments are stored in separated physical memory systems

Full events :
Full event data are stored into one physical memory system associated to a processing unit

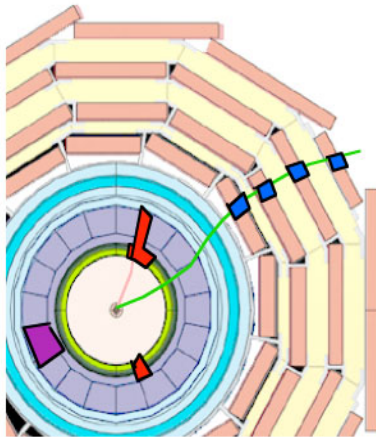
Hardware:

Fabric of switches for builder networks
PC motherboards for data Source/Destination nodes

Three Major issues: 1) Maximize link utilization (CHF); 2) Avoid bottleneck at outputs; 3) Assemble large number of ports



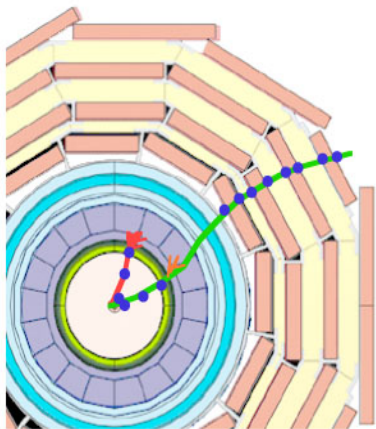
E.g. CMS two trigger levels



Level-1: Massive parallel processors 40 MHz synchronous

- Particle identification:
- high pT electron, muon, jets, missing ET
- Local pattern recognition and energy
- evaluation on prompt macro-granular information from calorimeter and muon detectors

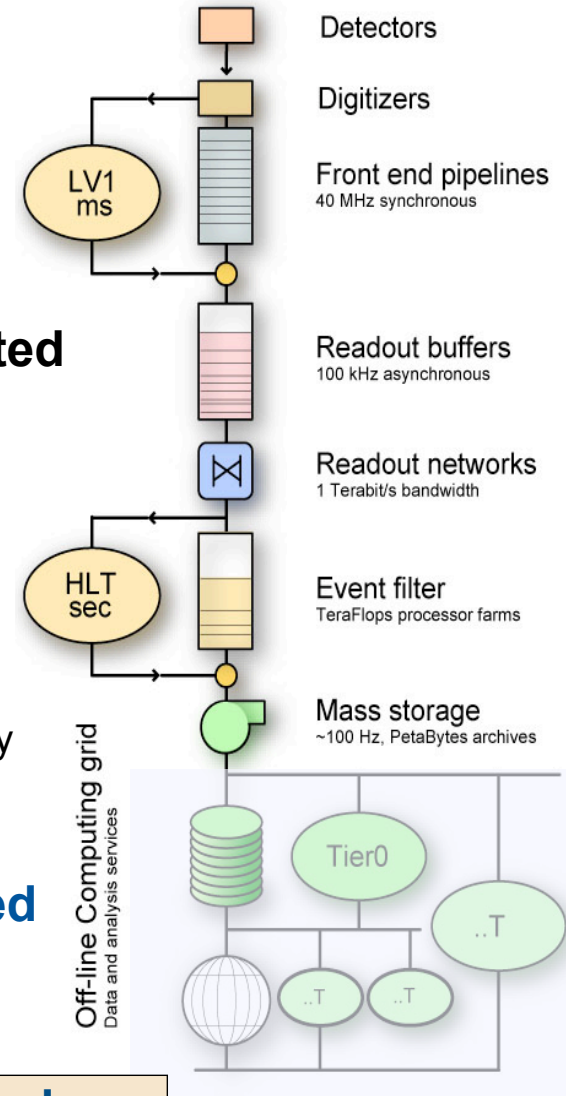
99.99 % rejected: 0.01 % Accepted



HLT: Full event readout into PC farms 100 kHz asynchronous farms

- Clean particle signature
- Finer granularity precise measurement
- Kinematics. effective mass cuts and event topology
- Track reconstruction and detector matching
- Event reconstruction and analysis

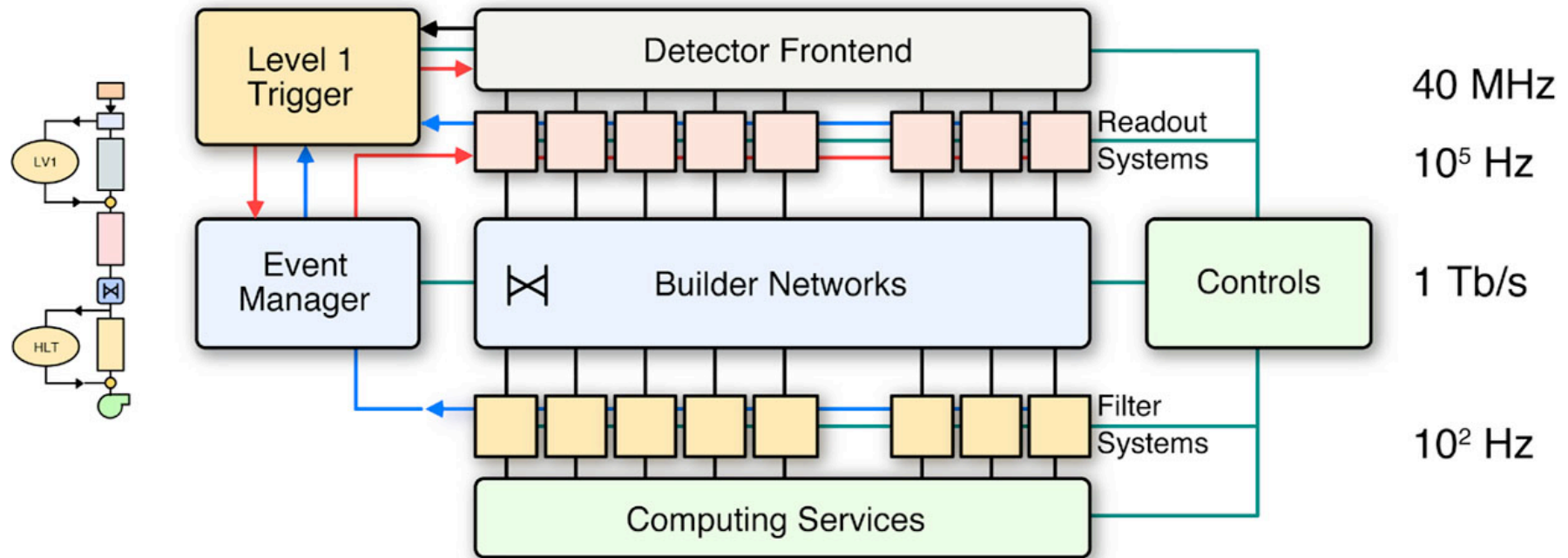
99.9 % rejected: 0.1 % Accepted



Total 99.999 % rejected 0.001 % Accepted



CMS DAQ baseline structure



Collision rate

Level-1 Maximum trigger rate

Average event size

Flow control&monitor

40 MHz

100 kHz

≈ 1 Mbyte

≈ 10⁶ Msg/s

Readout concentrators/links

Event Builder bandwidth max.

Event filter computing power

Event Builder GBE ports

Data production

Processing nodes

512 x 4 Gb/s

2 Tb/s

≈ **10 TeraFlop**

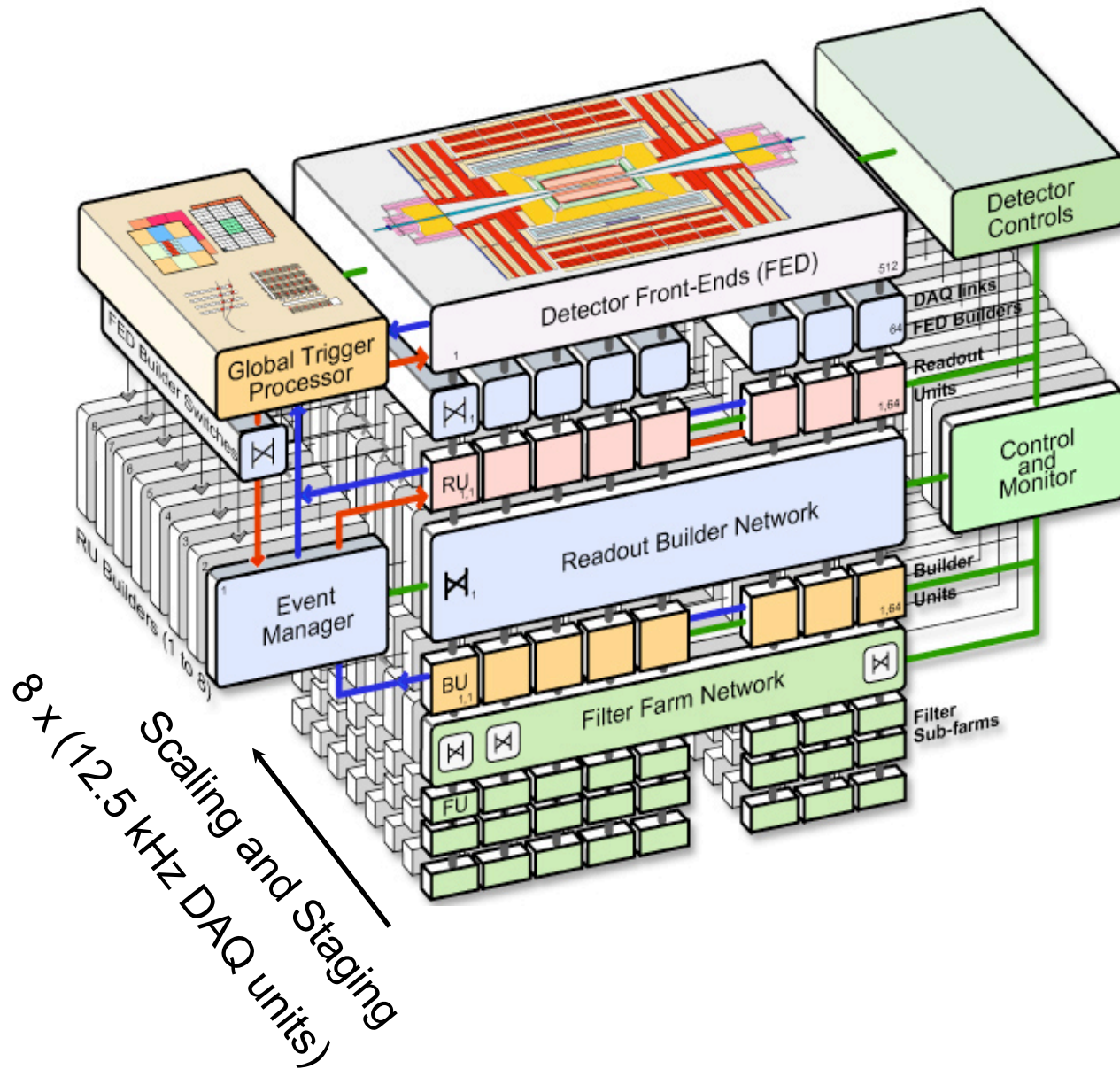
> **4000**

≈ Tbyte/day

≈ x Thousands



DAQ: scaling x 8 units



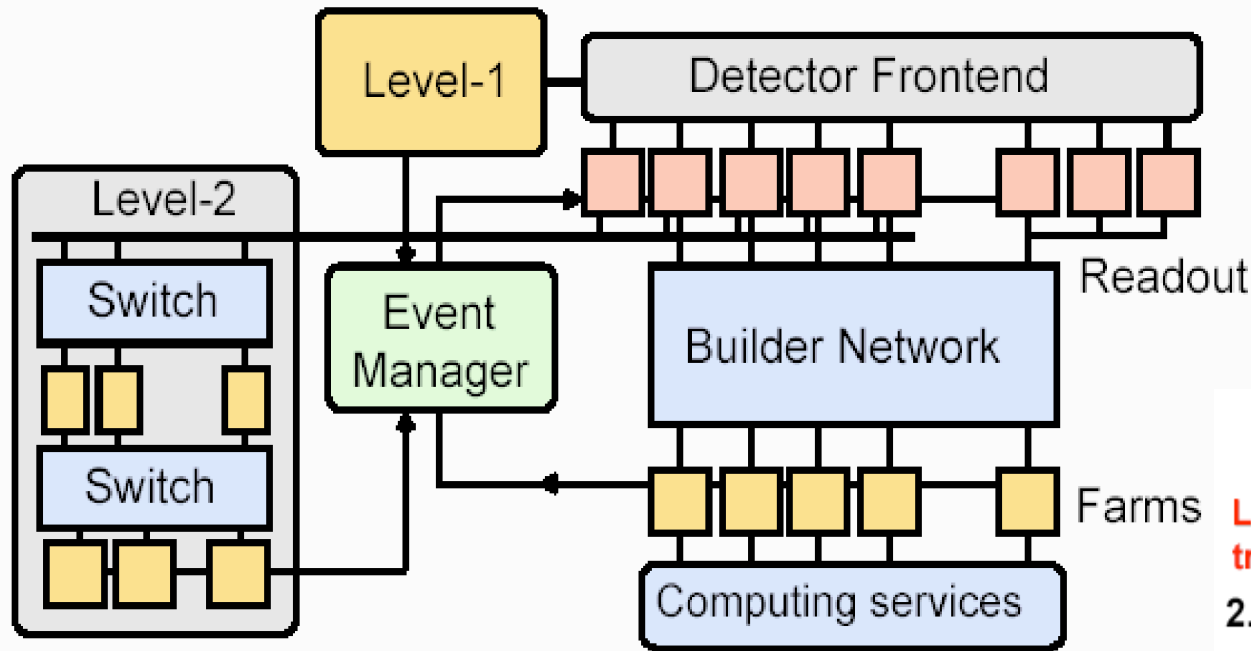
Data to surface:

Average event size	1 Mbyte
No. FED S-link64 ports	700
DAQ links (2.5 Gb/s)	512+512
Event fragment size	2 kB
FED builders (8x8 dual)	80
Technology(2004)	Myrinet

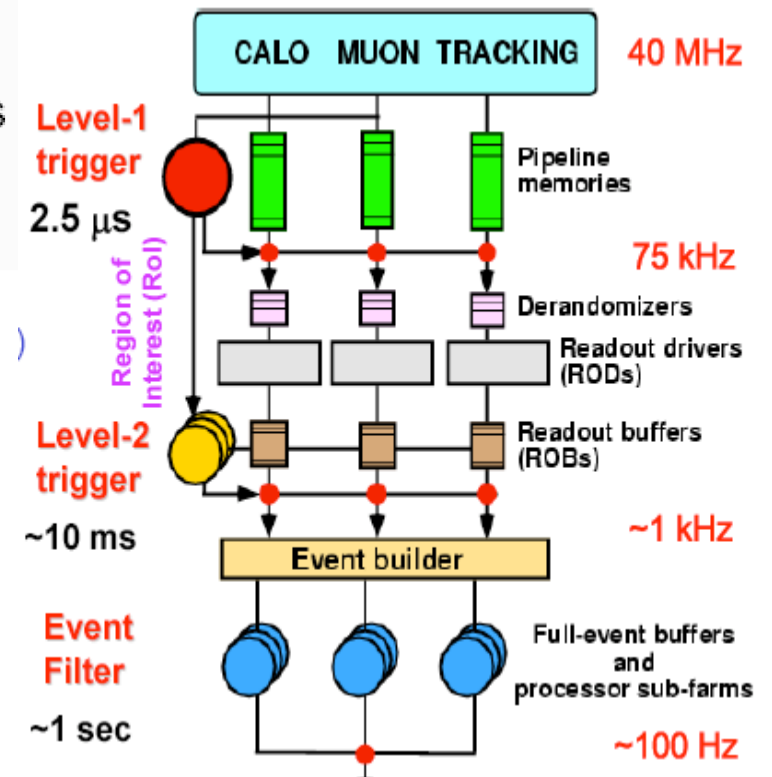
Readout Builder (x8):

Lv-1 max. trigger rate	12.5 kHz
GBE RU Builder 80x80x2	.125 Tb/s
Event fragment size	16 kB
RU/BU systems	80
Event filter power	~ TeraFlop
EVB technology	Ethernet

ATLAS DAQ Baseline Structure



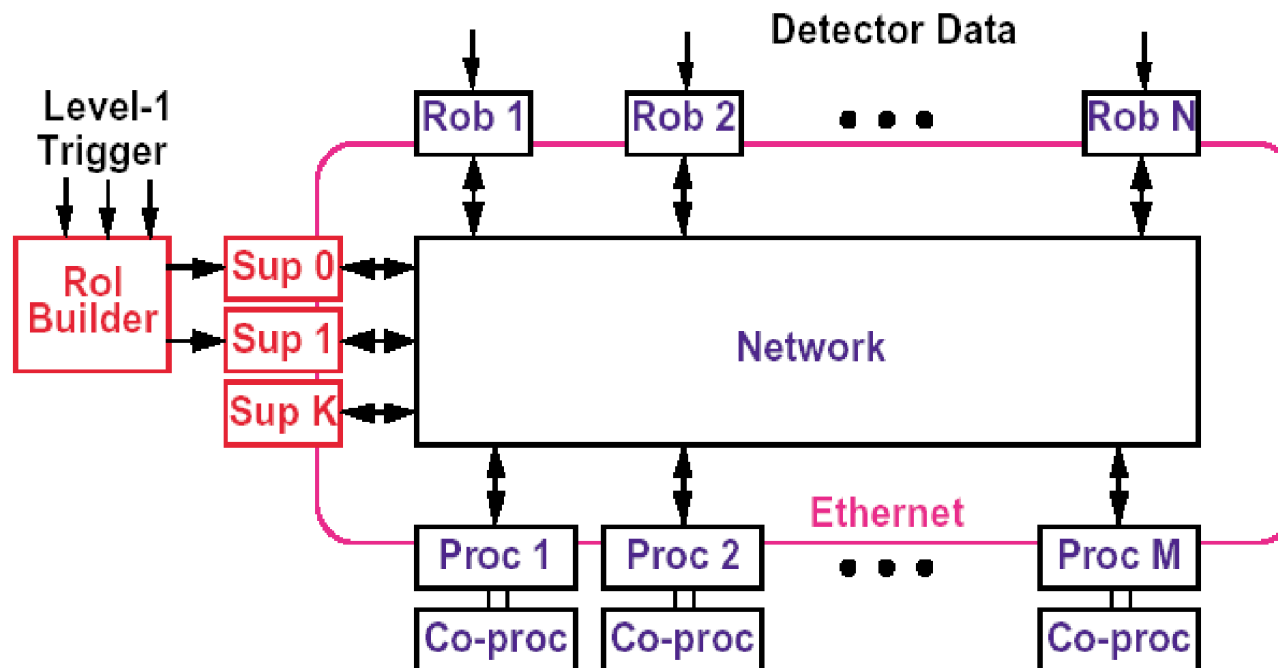
ROI Builder (From L1)
 Level-2 rejection factor: 100
 1600 Read Out Buffers (ROB)
 Supervisor Farm (@ 100 kHz)
 Input to Level-3 (~kHz)
 Event Builder: GB/s



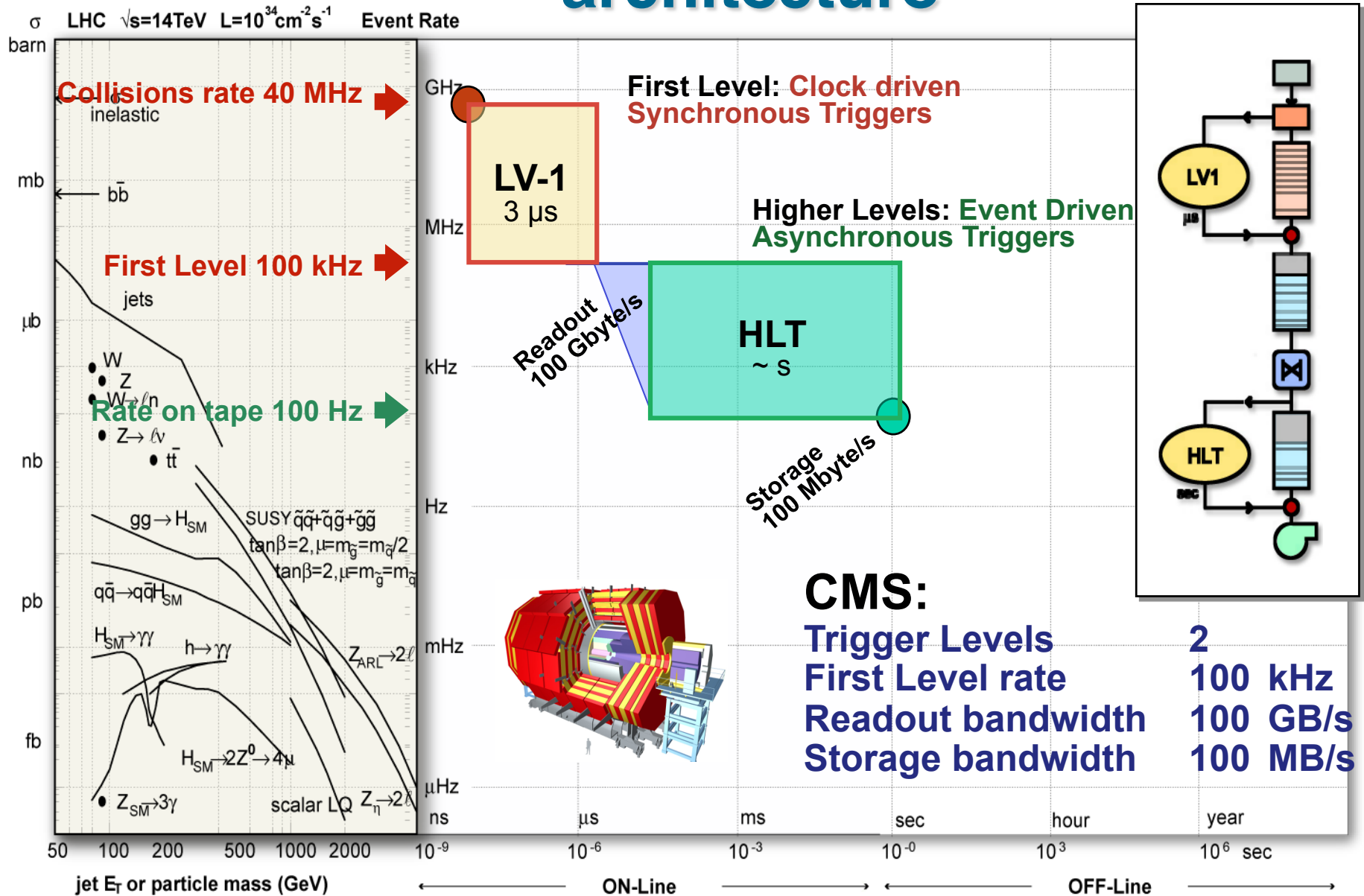
The Main Challenge: Level 2

■ Driven by Level-1 information

- ◆ Crucial parameters: data routing and CPU time (latency)
- ◆ ROIBuilder: custom hardware to combine ROI pointers
- ◆ Supervisor farm: collect info, allocate event to processor, distribute result to ROBs
- ◆ Processor farm: collect data from ROBs (upon request) execute algorithm; decision to Supervisor farm



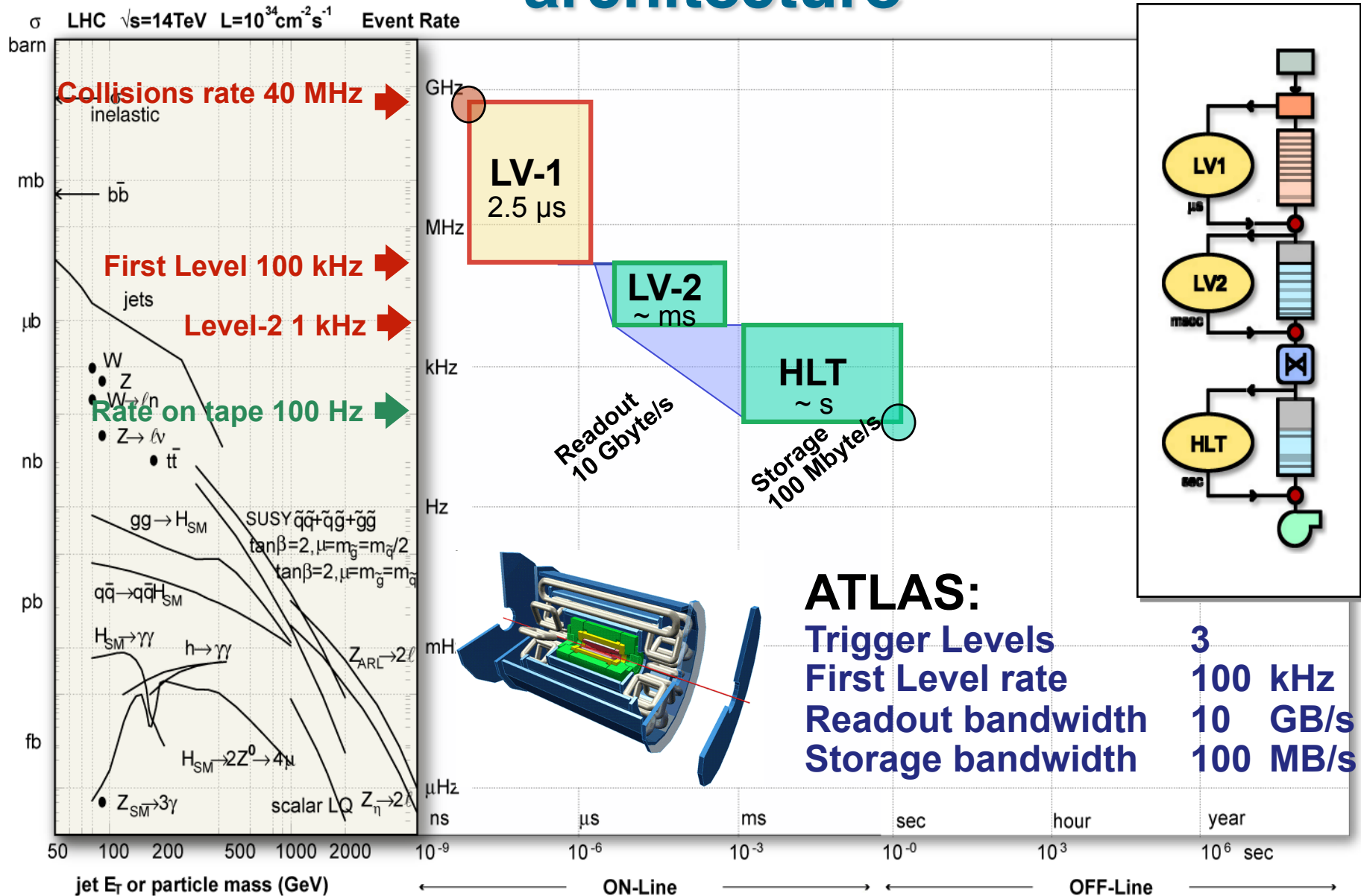
CMS trigger levels and DAQ architecture



CMS High Level Trigger

- **Rejection:**
 - 1:1000 selection
- **Algorithms:**
 - Algorithms can almost be as sophisticated as in offline analysis
 - Avoid unnecessary calculations; **reject as soon as possible**
 - Hence, internal “logical” trigger levels:
 - Level-2: use calorimeter and muon detectors
 - Level-2.5: also use tracker pixel detectors
 - Level-3: use of full information, including tracker
 - In principle continuum of steps possible
 - Regional reconstruction: e.g. tracks in a given road or region
- **Resources/CPU time:**
 - 100 kHz \rightarrow 10 μ s/event
 - If T_j is the time taken by the Level-J decision (J=2,3,...) and the rejection factors are R_j
$$T_{\text{tot}} = T_2 + T_3 / R_2 + T_4 / (R_3 R_2) + \dots$$
- **A 50 kHz system at startup will need ~2000 CPU's**

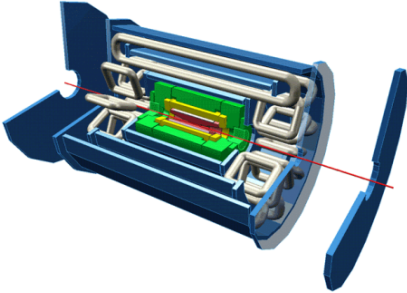
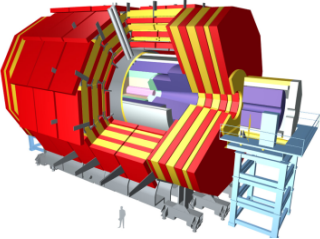
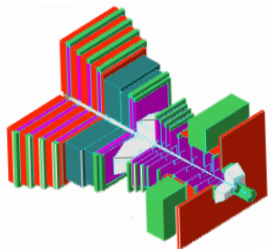
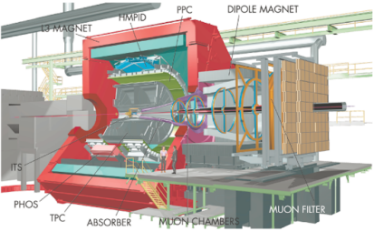
ATLAS trigger levels and DAQ architecture





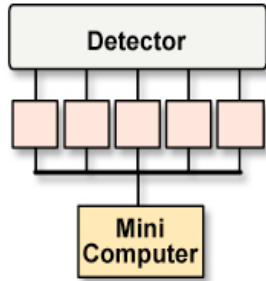
LHC trigger and DAQ summary



	No. Levels Trigger	Level-0,1,2 Rate (Hz)	Event Size (Byte)	Readout Bandw.(GB/s)	HLT Out MB/s (Event/s)
	3	LV-1 10^5 LV-2 3×10^3	1.5×10^6	4.5	300 (2×10^2)
	2	LV-1 10^5	10^6	100	O(1000) (10^2)
	2	LV-0 10^6	3×10^4	30	40 (2×10^2)
	4	Pb-Pb 500 p-p 10^3	5×10^7 2×10^6	25	1250 (10^2) 200 (10^2)

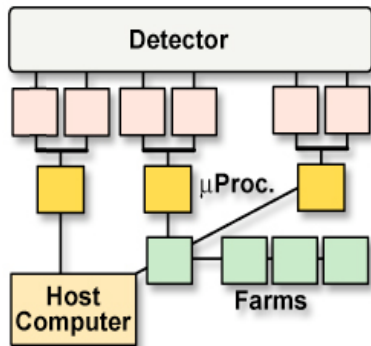
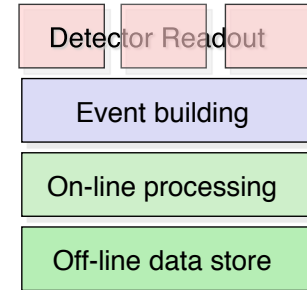


Evolution of DAQ structures with technologies



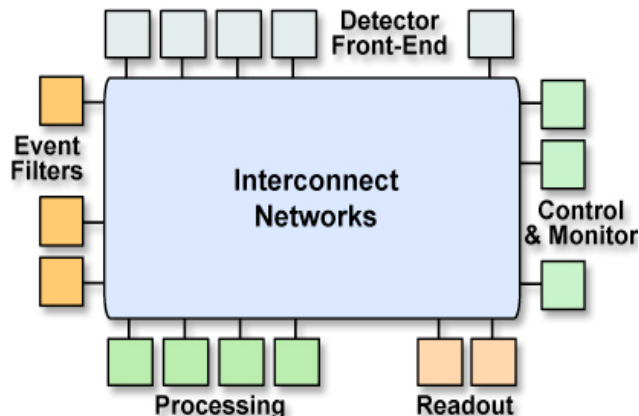
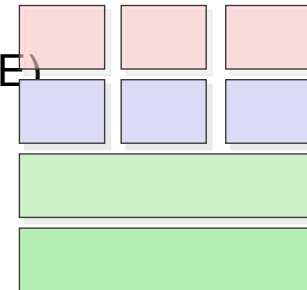
PS/ISR/SPS:1970-80: Minicomputers

Readout custom design
 First standard: CAMAC
 Software: noOS, Assembler
 • **kByte/s**



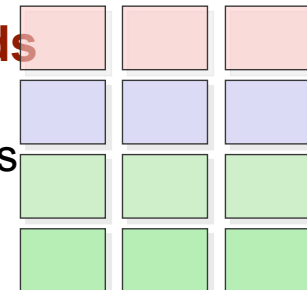
p-p/LEP:1980-90: Microprocessors

HEP proprietary (Fastbus), Industry standards (VME)
 Embedded CPU, servers
 Software: RTOS, Assembler, Fortran
 • **MByte/s**



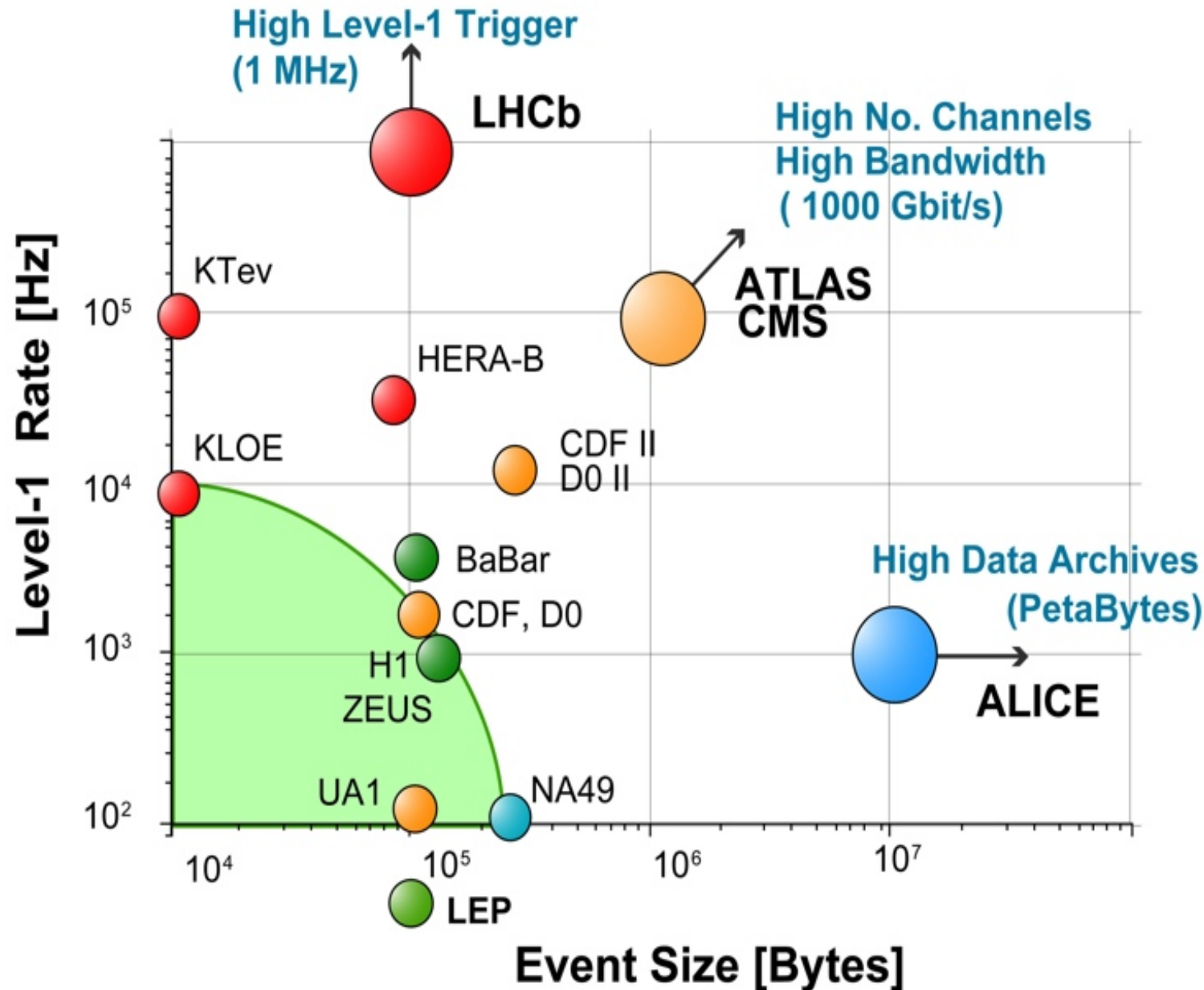
LHC: 200X: Networks/Clusters/Grids

PC, PCI, Clusters, point to point switches
 Software: Linux, C,C++,Java,Web services
 Protocols: TCP/IP, I2O, SOAP,
 • **TByte/s**





Trigger and data acquisition trends





DAQ operation: Control Room



Cessy: Master&Command control room

Fermilab: Remote Operations Center



CMS 2008



Meyrin: CMS DQM Center

CR: Any Internet access.....





Super LHC, DAQ upgrade



O(10) Luminosity increase (2014-16) will require:

- New front-end electronics and readout links
- Higher **level-1 selection power** (to maintain 100 kHz max. output)
- **Event builder (>10 Tb/s)** with an order of magnitude higher

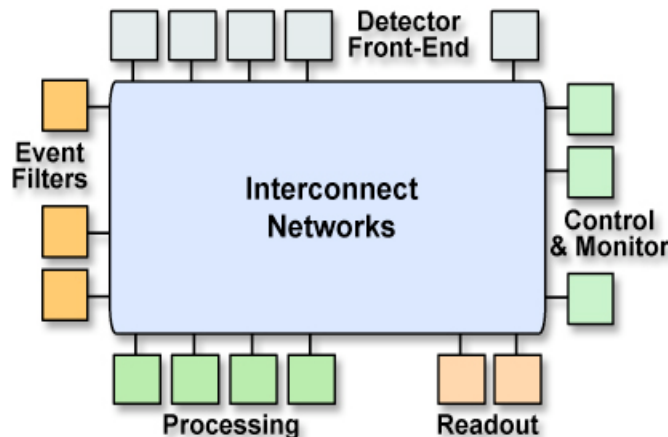
2014 SLHC. A possible DAQ design:

A **multi-Terabit/s network congestion free** and scalable (as expected from communication industry).

In addition to the Level-1 Accept, LV1 **Trigger transmits to the front-end readout units additional information such as the event type and the event destination IP address** that is the processing system (CPU, Cluster, TIER..) where the event has to be eventually built and analyzed.

The event fragment delivery and therefore the event building will be warranted by the network protocols and (commercial) network internal resources (buffers, multi-path, network processors, etc.)

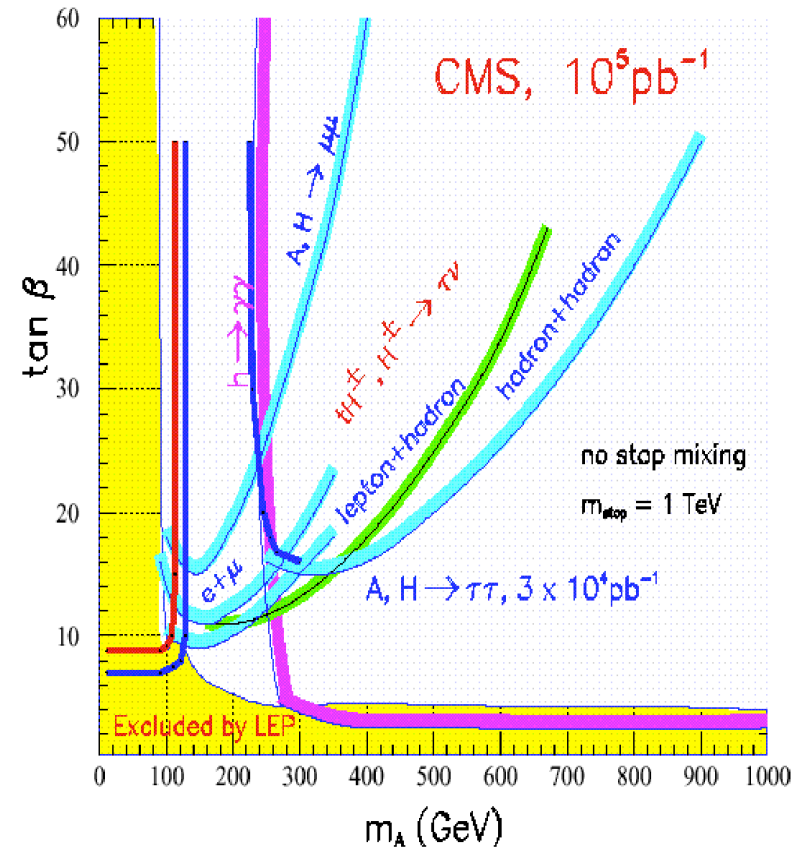
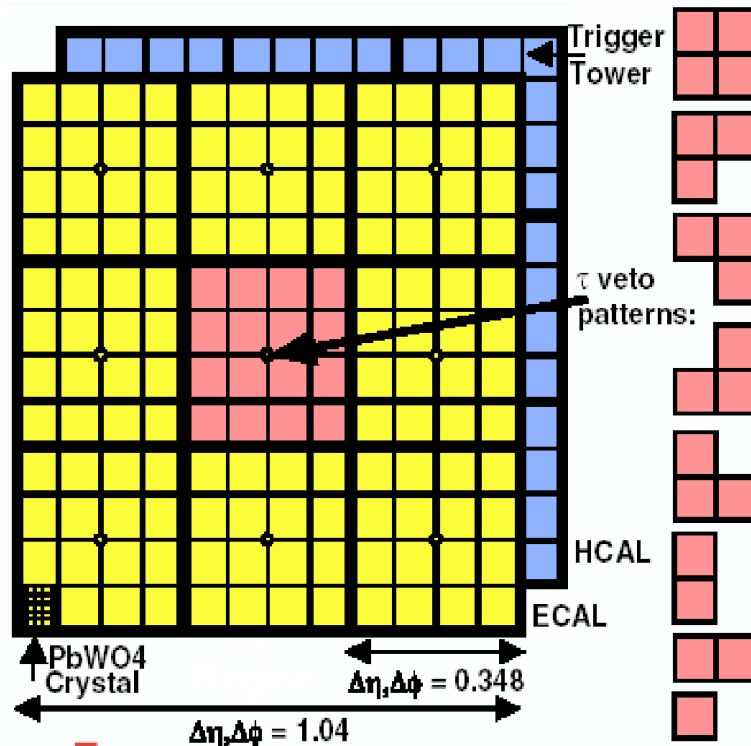
Real time buffers of Pbytes temporary storage disks will cover a real-time interval of days, allowing to the event selection tasks a better exploitation of the available distributed processing power.



**More
Slides**

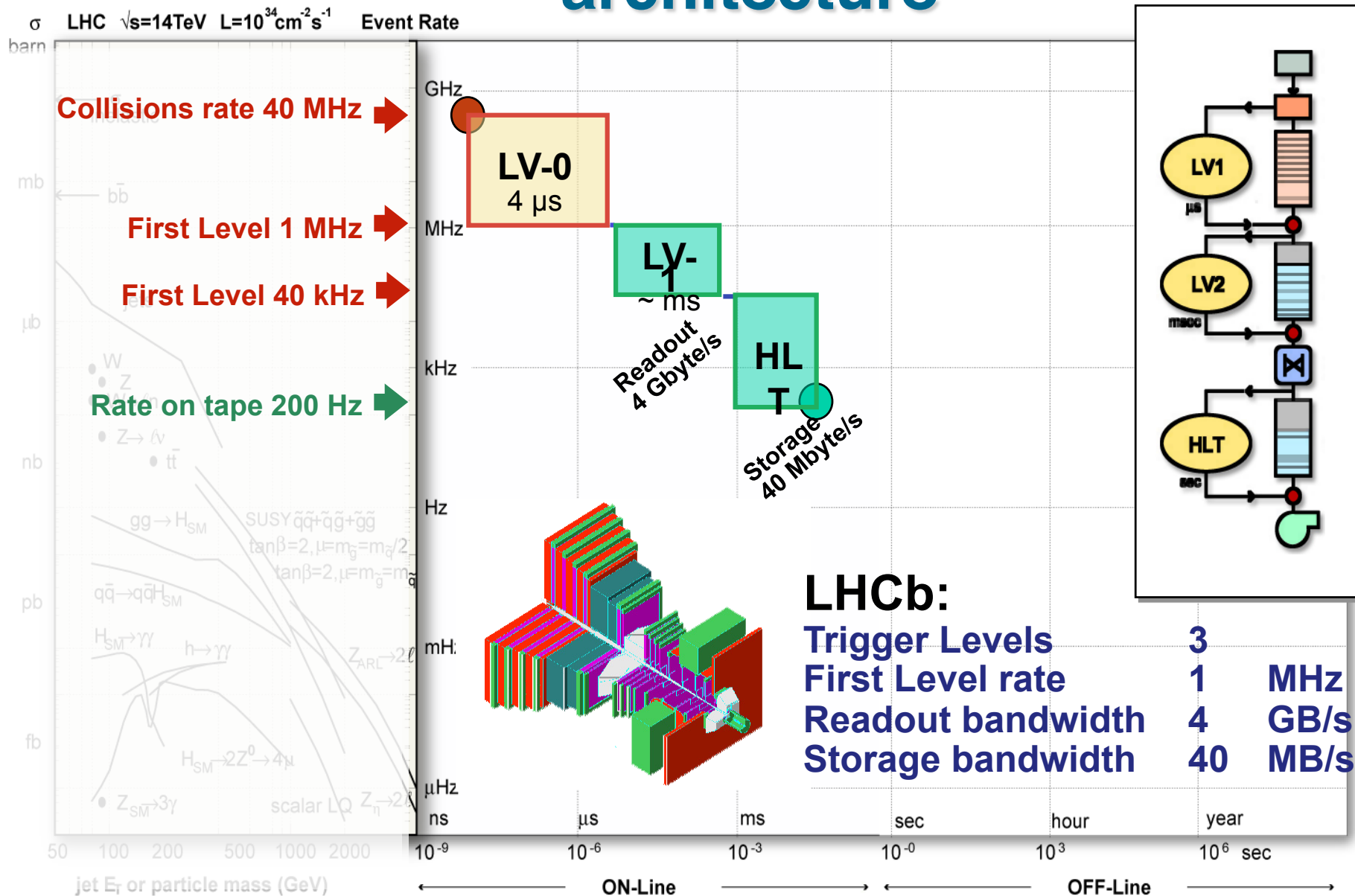
Taus

- ◆ Important signatures in SUSY
- **Tau trigger – CMS example**
 - ◆ Start with a jet
 - ◆ Require isolation
 - Actually tau-veto

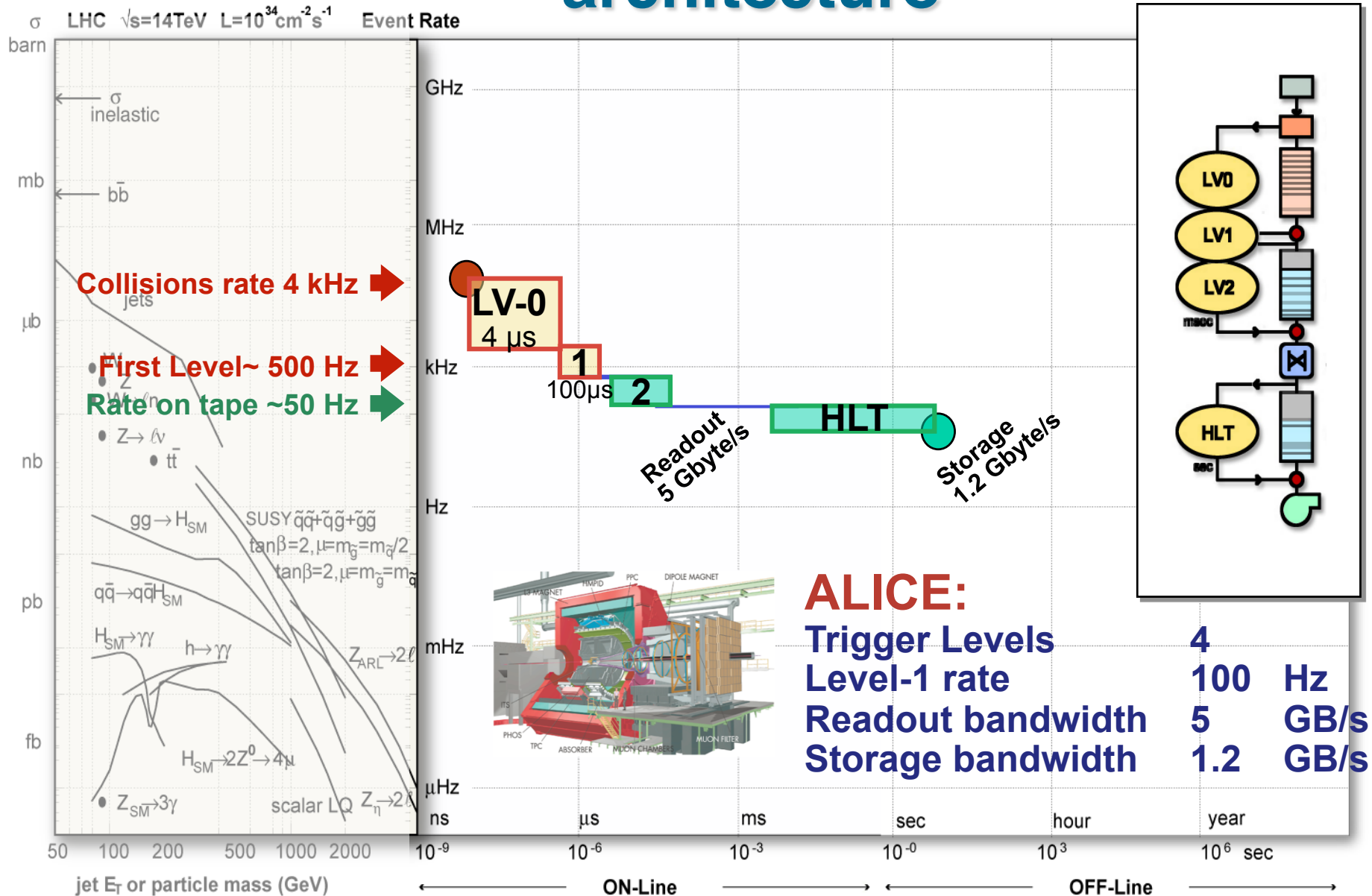


Jet = tau if all veto patterns in 4x4 are off

LHCb trigger levels and DAQ architecture



ALICE(Pb-Pb) trigger levels and DAQ architecture





Conclusions



12 yeas of R&D (too much?)

the project has lasted more or less a man generation from design to implementation...

Custom/Standards attention

Pay attention to maintenance and replacement issues. Survey new standards in the field of telecommunication, server packages, data centers, cooling etc.

Will we buy computing power and network bandwidth?

New kind of commodities: CPU power, memory, mass storage and bandwidth are becoming commercial products..

Configuration and control of complexity is an issue

Data taking efficiency depends on the real-time system performances but also on the prompt handling of all on-line resources. Configuration, fault tolerance, remote controls, monitor and security have to be improved.

Super LHC DAQ upgrade

The best R&D for the SLHC DAQ upgrade will come from the completion and operation of the current systems

Moore law "confirmed"

High energy physics experiments still provide "exceptional challenges" to data processing and data communication technologies, however in the majority of cases somebody else is driving the locomotive.

Level-1 trigger table (low/high lumi)

Low Luminosity

Total Rate: 50 kHz

Factor 3 safety,
allocate 16 kHz

Trigger	Threshold ($\epsilon=90-95\%$) (GeV)	Indiv. Rate (kHz)	Cumul rate(kHz)
1e/ γ , 2e/ γ	29, 17	4.3	4.3
1 μ , 2 μ	14, 3	3.6	7.9
1 τ , 2 τ	86, 59	3.2	10.9
1-jet	177	1.0	11.4
3-jets, 4-jets	86, 70	2.0	12.5
Jet * Miss- E_T	88 * 46	2.3	14.3
e * jet	21 * 45	0.8	15.1
Min-bias		0.9	16.0

High Luminosity

Total Rate: 100 kHz

Factor 3 safety,
allocate 33.5 kHz

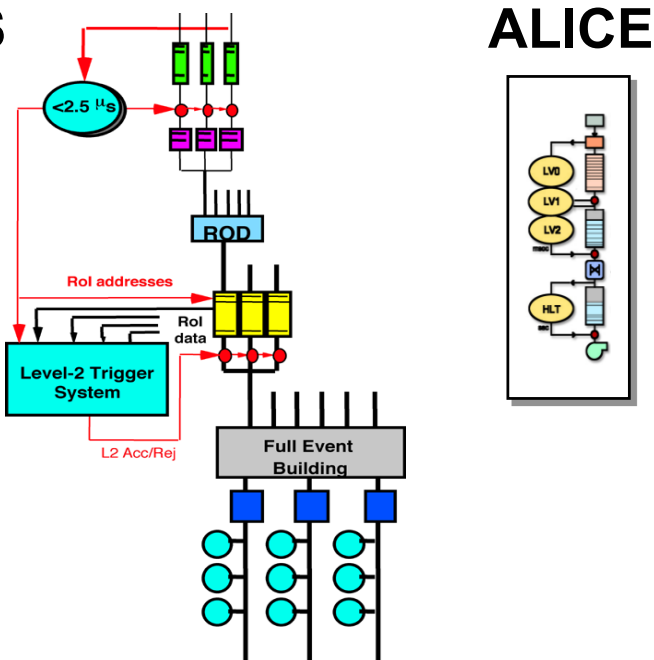
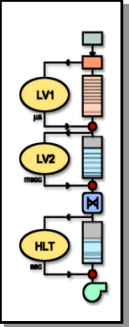
Trigger	Threshold ($\epsilon=90-95\%$) (GeV)	Indiv. Rate (kHz)	Cumul rate (kHz)
1e/ γ , 2e/ γ	34, 19	9.4	9.4
1 μ , 2 μ	20, 5	7.9	17.3
1 τ , 2 τ	101, 67	8.9	25.0
1-jet	250	1.0	25.6
3-jets, 4-jets	110, 95	2.0	26.7
Jet * Miss- E_T	113 * 70	4.5	30.4
e * jet	25 * 52	1.3	31.7
μ * jet	15 * 40	0.8	32.5
Min-bias		1.0	33.5

Technologies in Level-1 trigger systems

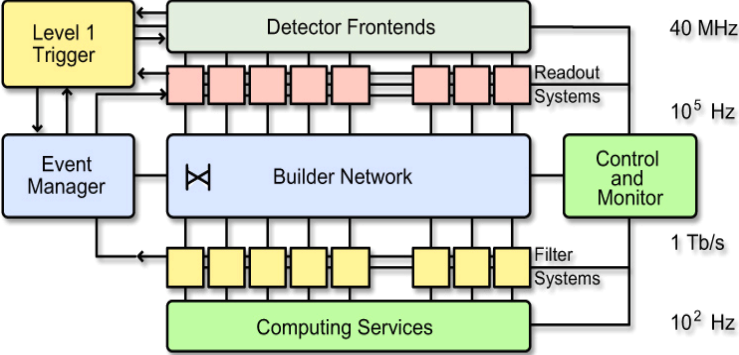
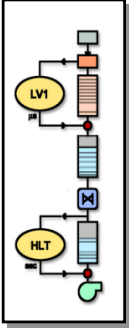
- ASICs (Application-Specific Integrated Circuits) used in some cases
 - ◆ Highest-performance option, better radiation tolerance and lower power consumption (a plus for on-detector electronics)
- FPGAs (Field-Programmable Gate Arrays) used throughout all systems
 - ◆ Impressive evolution with time. Large gate counts and operating at 40 MHz (and beyond)
 - ◆ Biggest advantage: flexibility
 - Can modify algorithms (and their parameters) in situ
- Communication technologies
 - ◆ High-speed serial links (copper or fiber)
 - LVDS up to 10 m and 400 Mb/s; HP G-link, Vitesse for longer distances and Gb/s transmission
 - ◆ Backplanes
 - Very large number of connections, multiplexing data; operating at ~160 Mb/s

DAQ structures at LHC

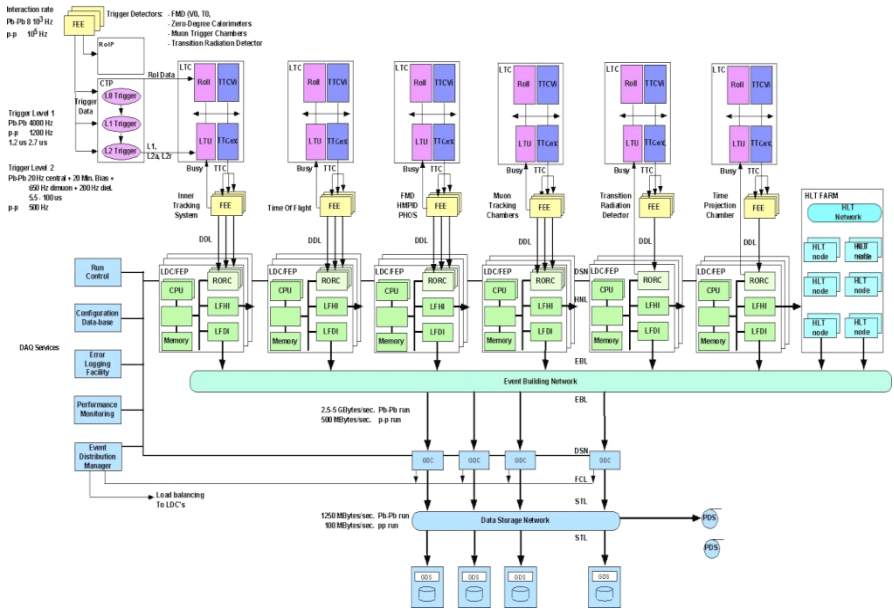
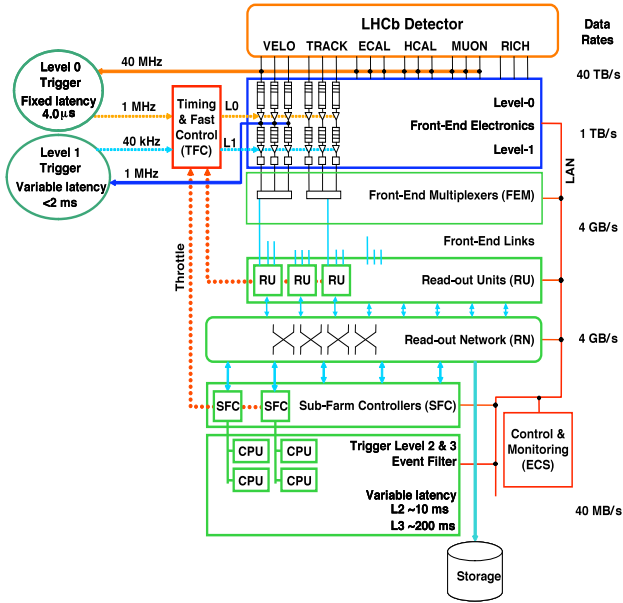
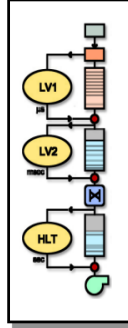
ATLAS



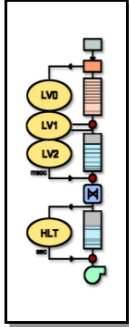
CMS



LHCb

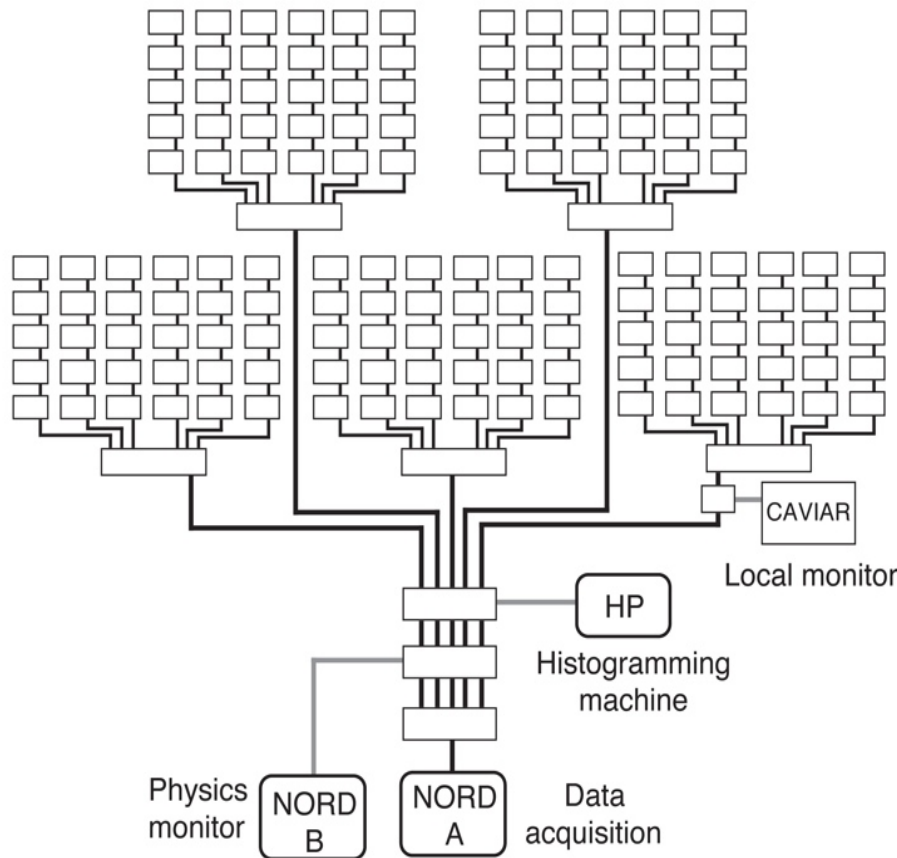


ALICE



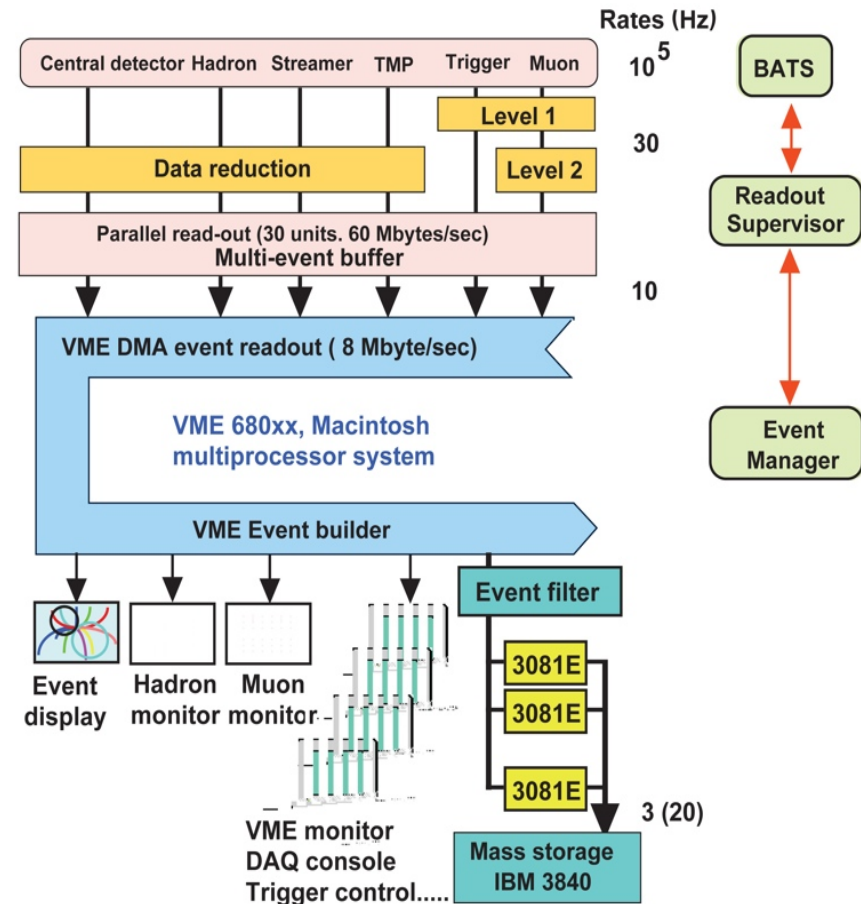


1978-1989. UA1 DAQ system (0.1 MHz, 30 Hz)



1981-84

- Remus data acquisition (≈ 200 CAMAC crates)
- rate on tape ≈ 1 Hz (event size ≈ 100 Kbyte)



1985-1989

VME, IBM-emulators, Desktops

Proprietary/Standards: CAMAC, embedded μ p, emulators, VME