Experimental techniques in high-energy nuclear and particle physics

"Dottorato di Ricerca in Ingegneria dell'Informazione"

LECTURE 7.

Electronics

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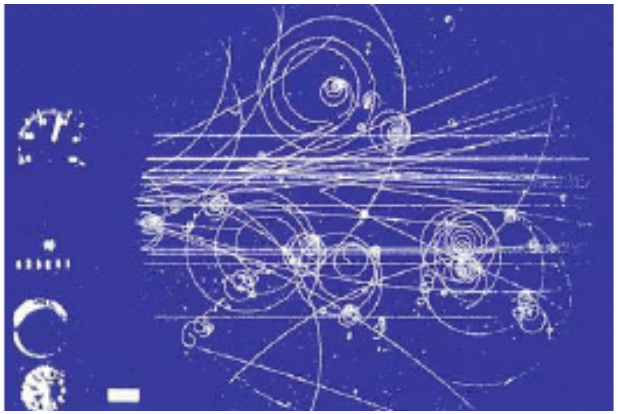
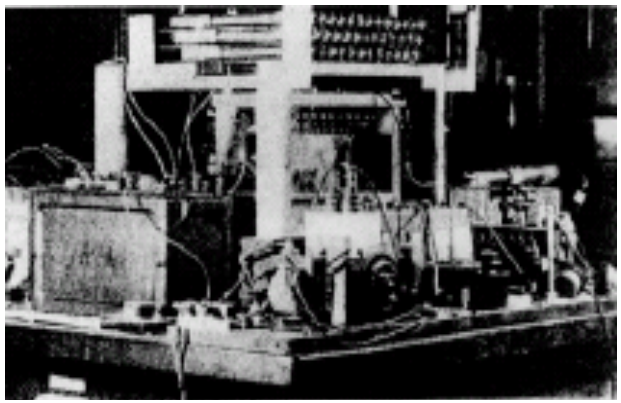
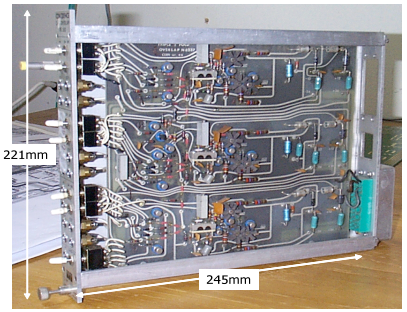
Historical evolvement

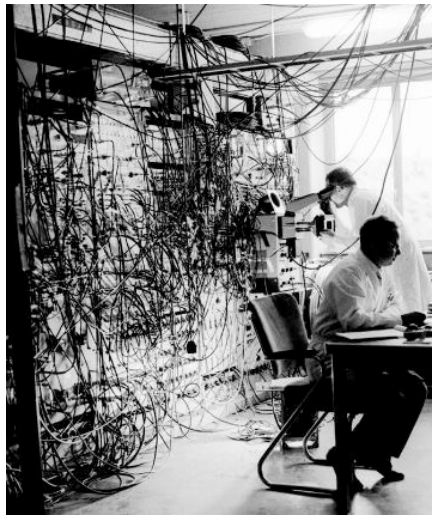
- Electronics has been the enabling technology that has allowed the development of modern HEP detectors.
- First particle detectors relied on direct eye observation (and films)
  - Phosphorus screen, cloud chamber, Bubble chamber, Spark chamber
- The use of electronics has allowed the development of a large multitude of detector types
  - Scintillators with PM or APD's, gas detectors, liquid detectors (liquid Argon), solid state (silicon), ,

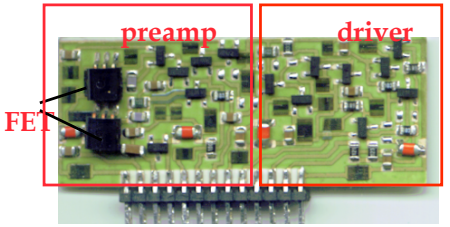


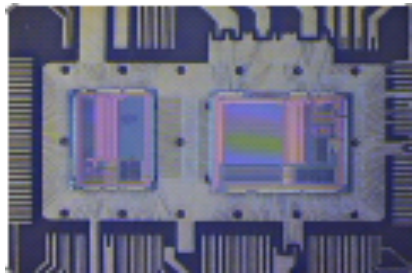


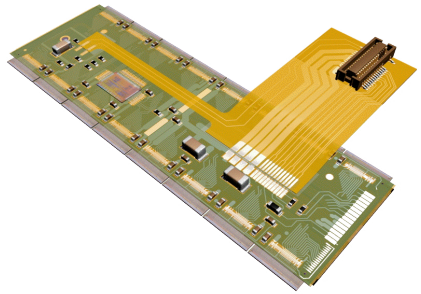
- Use of basic amplifiers with analog oscilloscope displays
- Use of modular electronics with digital computer interfaces
- Use of discrete front-end electronics within detector
- Use of highly integrated custom front-end electronics with digital signal processing and massive high speed connections to large computer farms

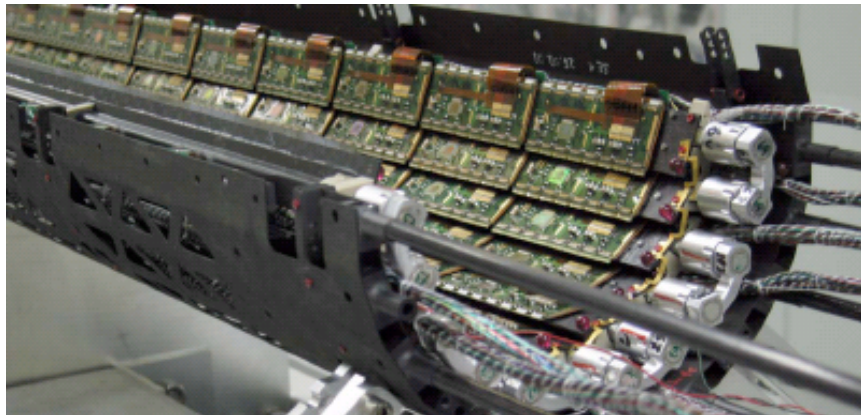






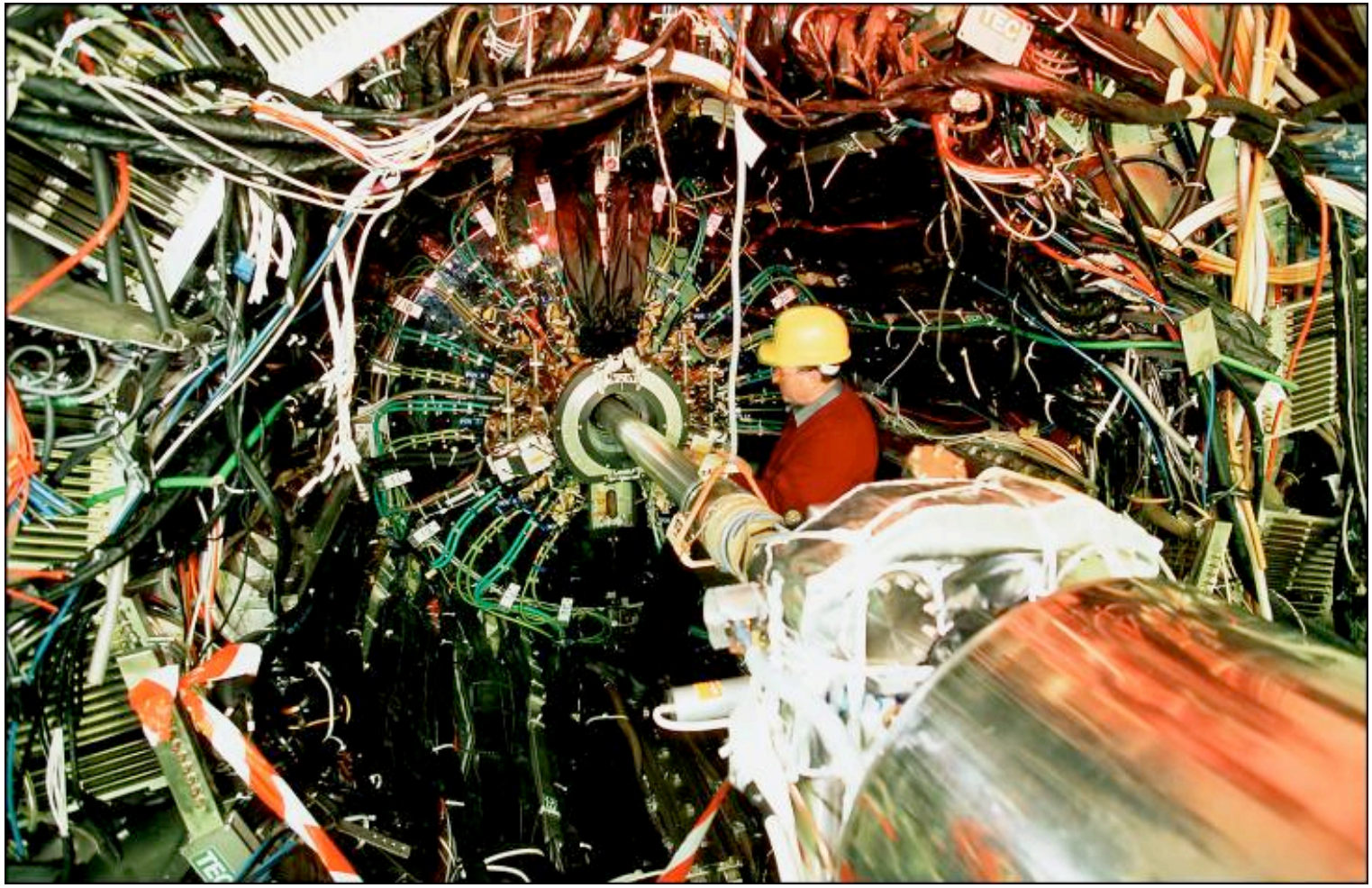




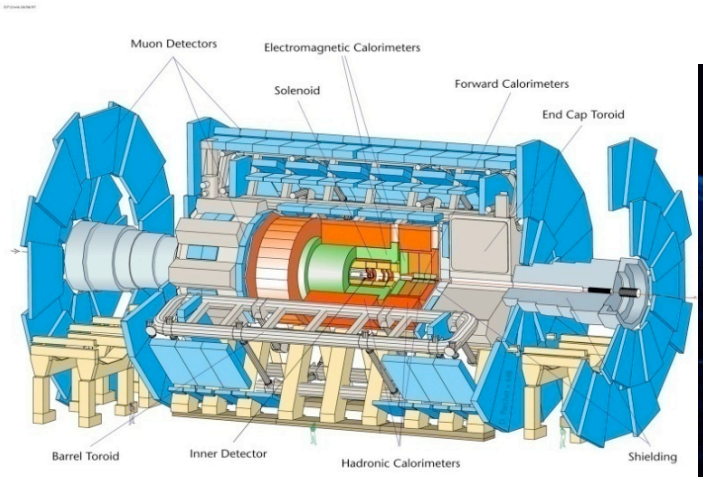


Electronics in experiments

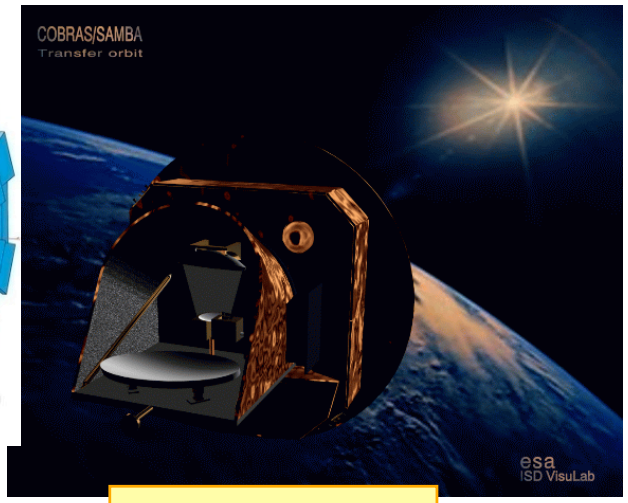
- A lot of electronics of different kind in the different experiments…
  - Readout electronics : amplification, filtering… : Analog electronics (A,V,C)
  - Processing & Trigger electronics : Digital electronics (bits)
  - The performance of electronics impacts on the detector performance



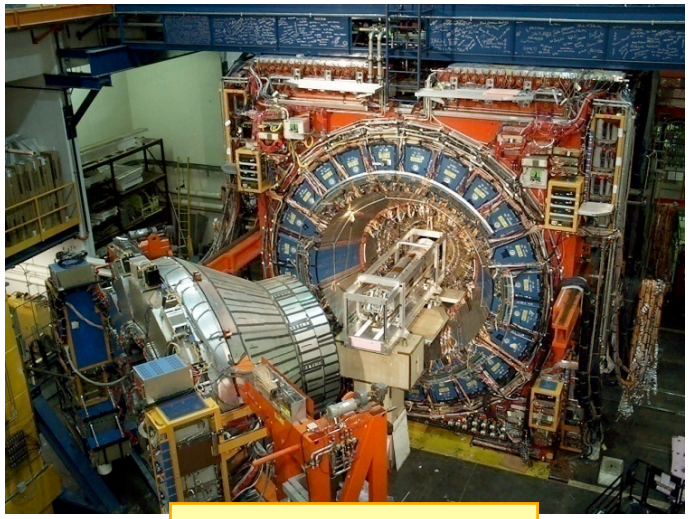
A large variety of detectors…



ATLAS : Higgs boson

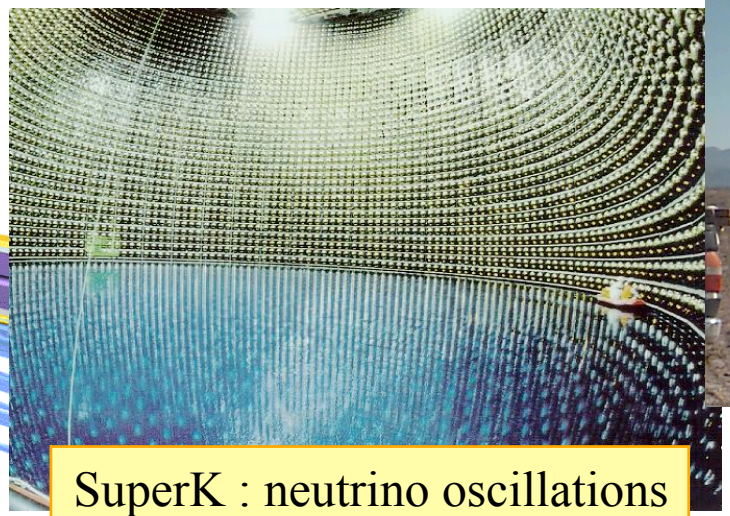


Planck : CMB



CDF : top quark

CMS:Higgs boson

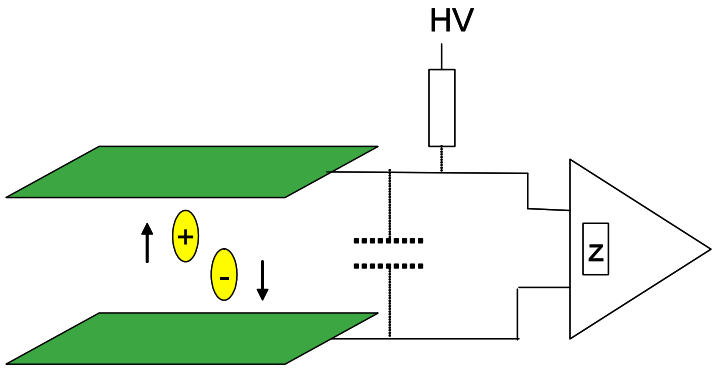


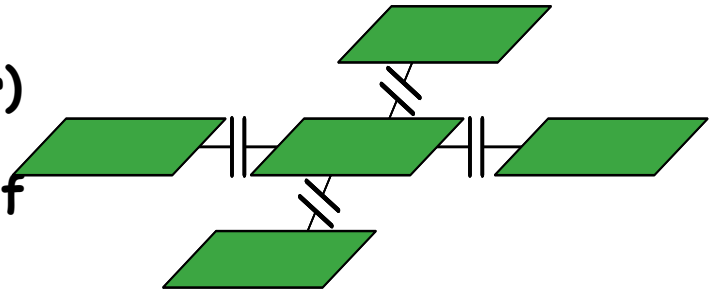
SuperK : neutrino oscillations

AUGER : cosmic rays 10^{20}eV

Signals from detectors

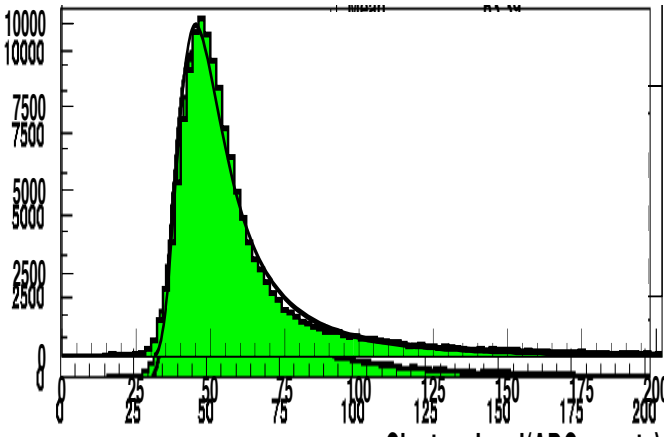
- Detector generates basic signal (charge) from ionization in gas, liquid or solid state (or photo electrons) with detector "gain" in some cases (gas, PM)
- The detector can from an electronics point of view be considered as a simple capacitor (with some possible leakage and a simple HV biasing circuit).
  - Induced signal modeled as current source
- The signal shape (charge collection) depends on the details of the detector
  - Normally relatively fast rising edge
  - May possible have a slow tail (ion tail in gas detectors)
- Typical signal is a few femto coulombs (e.g. 22ke=4fC in 300μm silicon detector)
- In an open detector with 10pf capacitance this gives a voltage buildup of only few hundred μV
- There are in most cases also significant capacitive coupling to neighbor detector channels

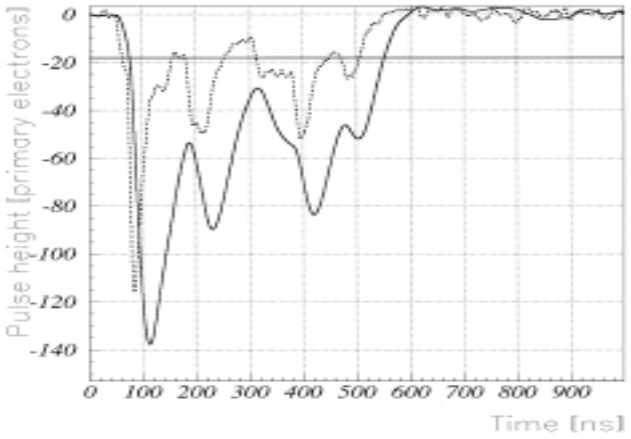




Detector signal

- Traversing particles deposit randomly different signals in tracking detectors
  - Landau distribution for silicon detectors with a given "minimum" MIP (minimum ionizing particle: ~20ke in 300μm silicon)
- Signal may consist of multiple sub-pulses for one particle
  - Drift tubes with clusters originating from individual primary ionizations in gas
  - One would like to detect first cluster or "merge" all into one signal with "constant" shape
- Measurement of energy (calorimeters)
  - Measurements over large linear range with high resolution



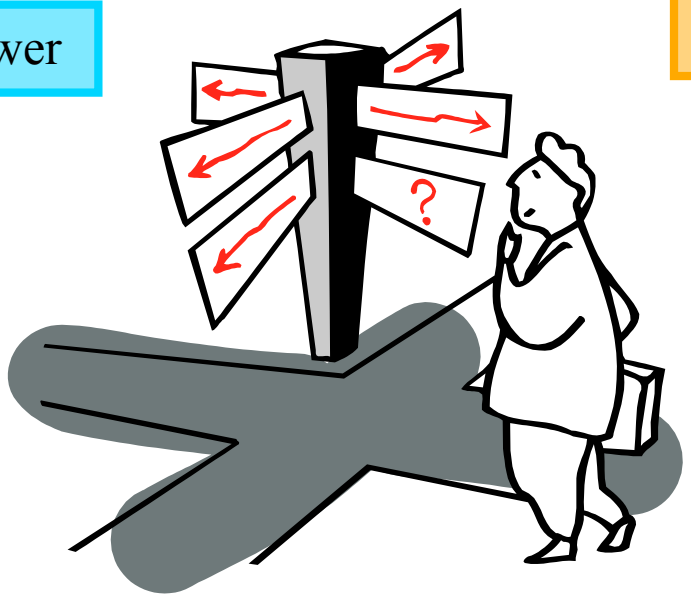


Readout electronics : requirements

Low noise

Low power

High speed



High reliability

Large dynamic range

Radiation hardness

Low cost !
(and even less)

Low material

Issues for large systems

- Performance
- Power consumption
- Circuit size
- Programmability & ease of control
- Uniformity
- Quality (Yield = fraction of working circuits)
- Testability

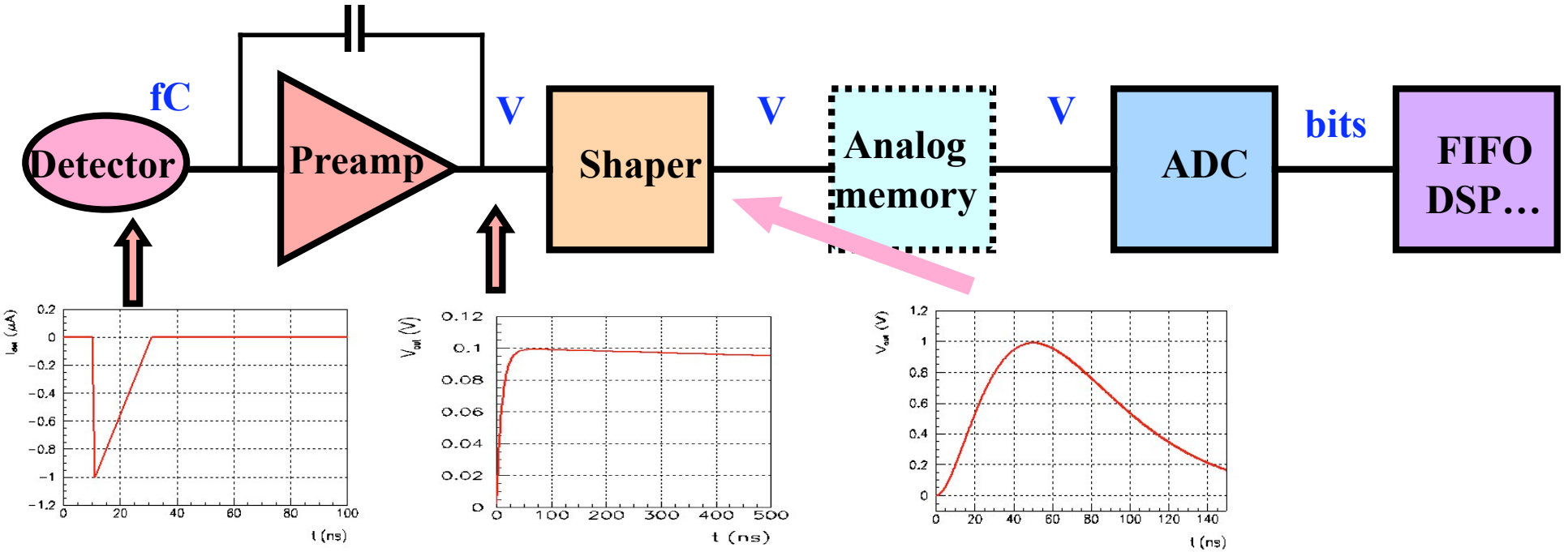
- Translate into choice of technology, cost, impact on detector, flexibility and ease of use,…

Requirements for LHC experiments

- Not all requirements are identical to LHC but the experiments exemplify many of the choices
  - Not easy to generalise without examples
- Major elements
  - Front end readout - amplification and storage
  - Off-detector readout
  - Data transfer
  - Power provision
  - Control, safety, monitoring
- Ideally, design a system - including all interconnections
  - In reality, we typically address the interesting or challenging questions first, trying to specify as well as possible the important constraints
  - However, when problems emerge they are often traceable to system issues

Overview of readout electronics

- Most front-ends follow a similar architecture
  - Pre-amplifier interfacing to detector
  - Shaping – filtering
  - Further treatment



- Very small signals (fC) -> need amplification
- Measurement of amplitude and/or time (ADCs, discris, TDCs)
- Several thousands to millions of channels

Detector technologies for tracking

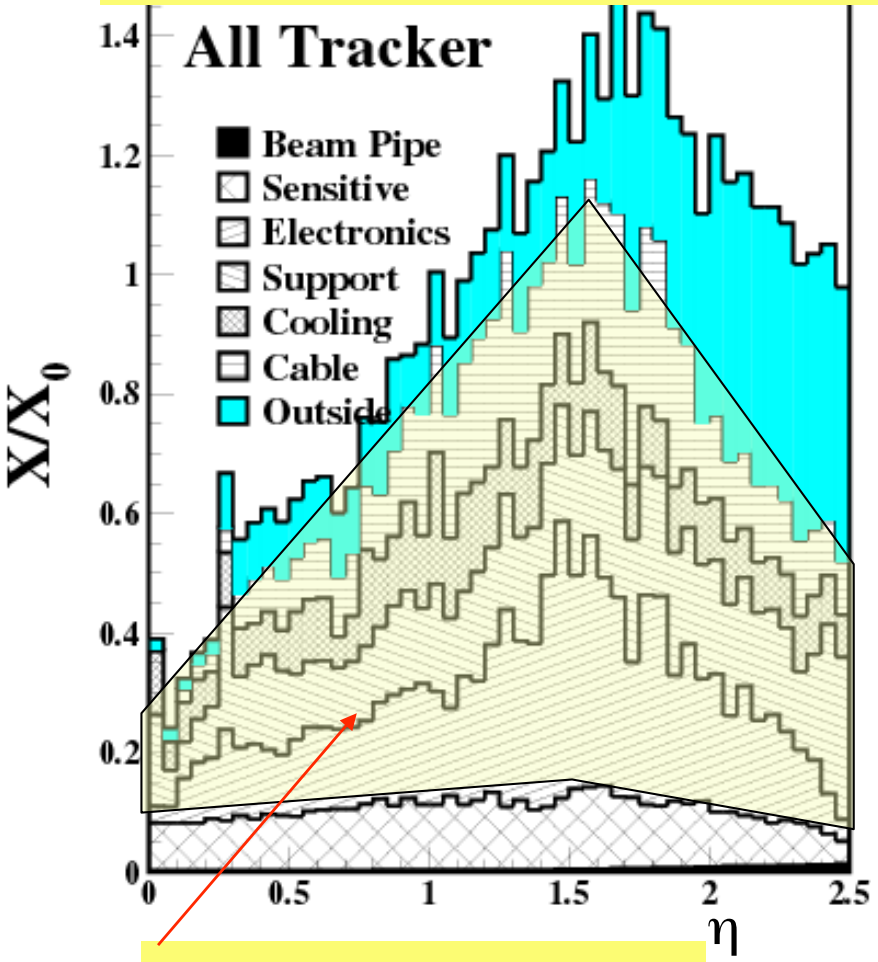
- tracking systems typically built from
  - Silicon
    - Pixels & CCDs
    - Silicon microstrips
    - Silicon drift detectors
  - Gaseous detectors
    - TPC, large volume drift chambers
    - planar wire chambers, MSGC, GEM,…
    - straw tubes
  - Occasionally… scintillating fibre

  - Sensor parameters not identical but often similar
    - Signal size ~ 25,000 electrons (~2000 - 100,000e)
    - Collection time ~few x10ns, but may have slow components
    - Electrical parameters: capacitance, resistance, leakage currents
    - Other factors - discharge protection,…

Impact of power on detector

- Ideally, minimise material by low power but heat dissipated by circuits is only part of the problem
  - CMS SST front end power: ~10M x 2-3mW = 20-30kW
- Long resistive cables typically consume more power than active electronics
  - Add weight, require cooling,..
- Consequent impact on material budget, especially for interior regions of experiment
- Can voltage regulators be used in the system?
  - If so it may be possible to bring in power at higher voltage, reducing currents in cables

Material budget in CMS Tracker



All electronics related

LHC parameters

- Major factors which influence electronics design and implementation

directly

- Clock speed
- Storage time
- Readout rate
- Granularity
- Data volume

indirectly

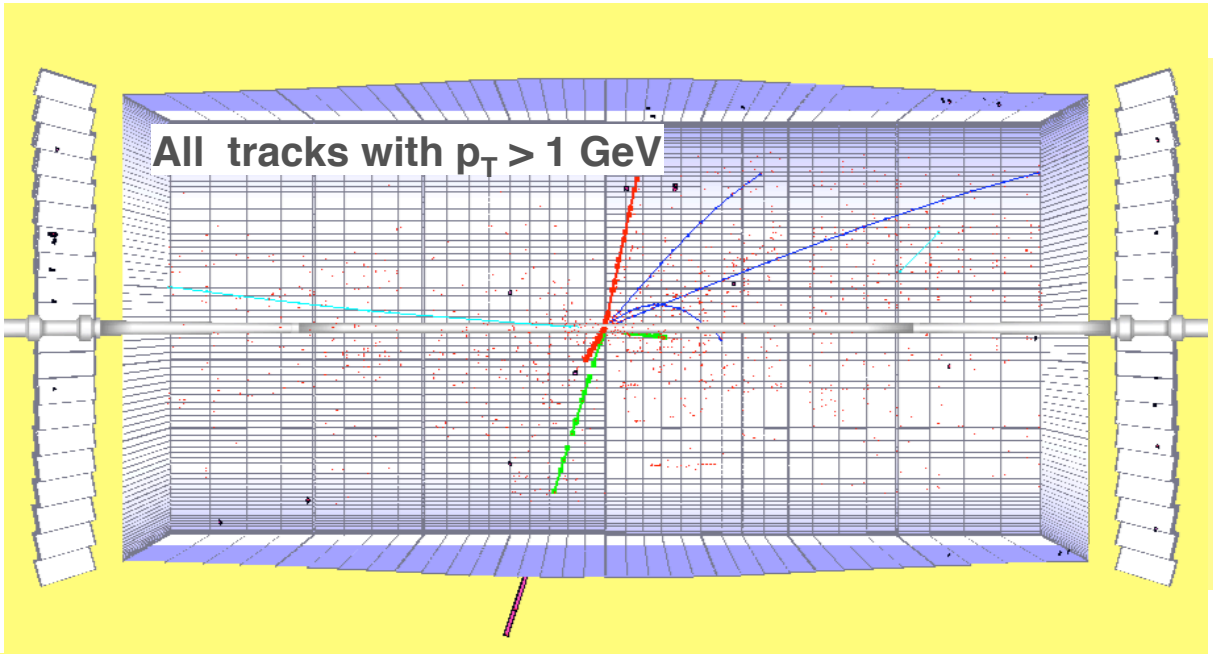
- Integrated L **(radiation)**
- Operating temperature
- T stability

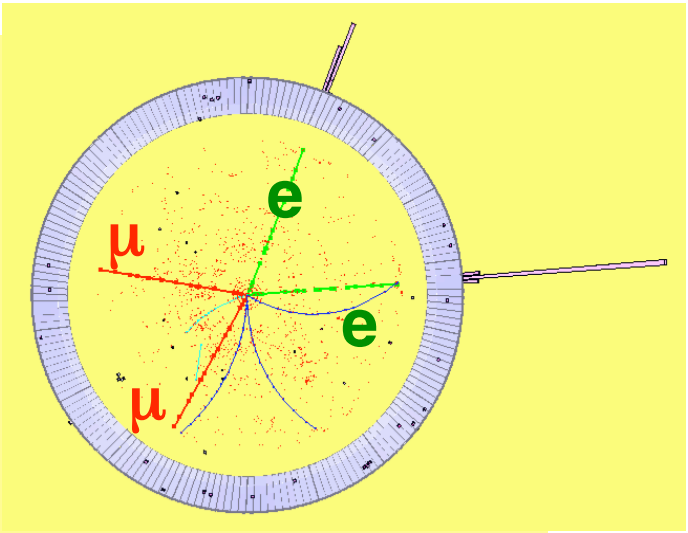
implied

- Operating voltages
- **Power**
- Performance

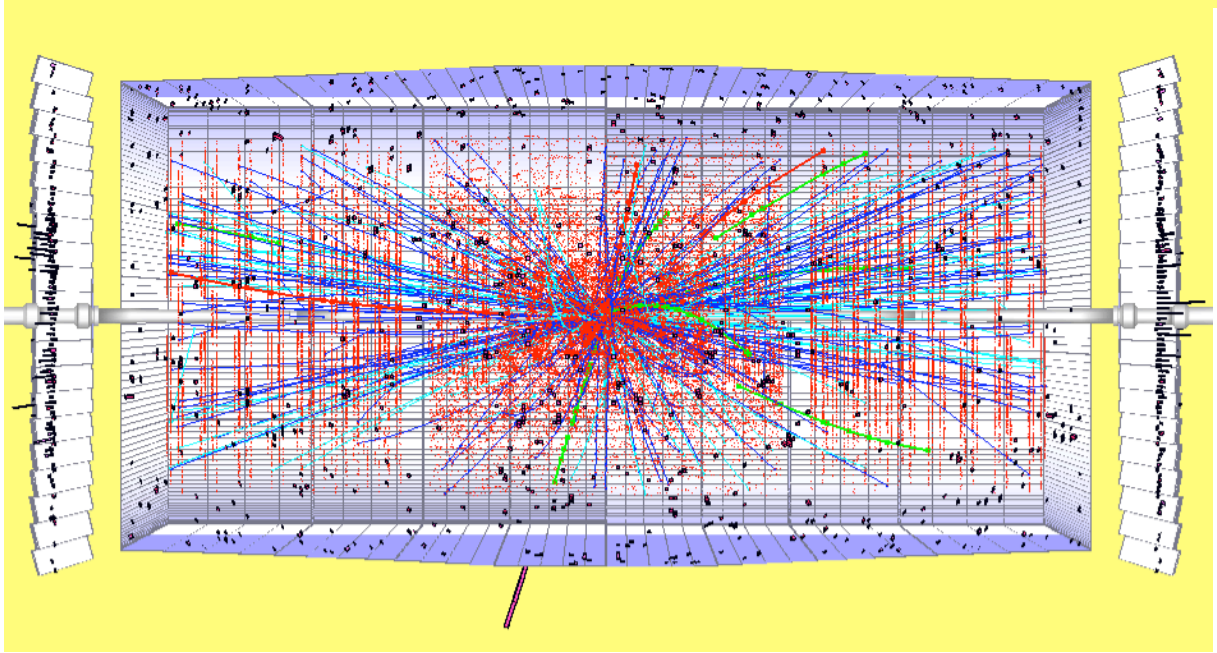
	p-p	**Pb-Pb**
Luminosity	10^{34} cm^{-2}s^{-2}	10^{27} cm^{-2}s^{-2}
Annual integrated L	5x10^{40} cm^{-2}	
CM Energy	14 TeV	5.5 TeV/N
$\sigma_{inelastic}$	~70mb	~6.5b
Interactions/bunch	~20	0.001
Tracks/unit rapidity	~140	3000-8000
Beam diameter	20μm	20μm
Bunch length	75mm	75mm
Beam crossing rate	40MHz	8MHz
Level 1 trigger delay	≈3.2μs	≈3.2μs
Mean L1 trigger rate	<100kHz	<8kHz

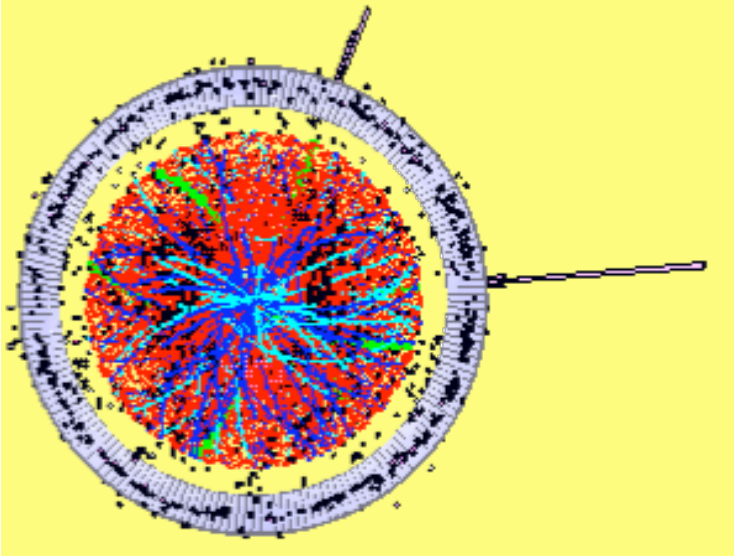
What a luminosity of $10^{34}cm^{-2}s^{-1}$ means on Tracking ...





H →ZZ* → 2e2μ



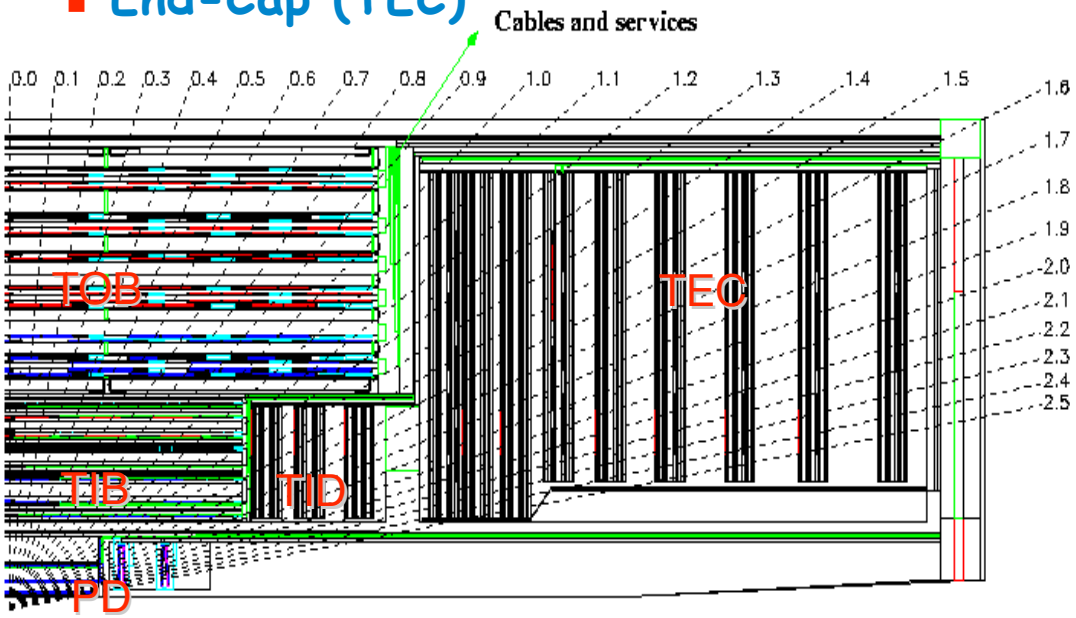


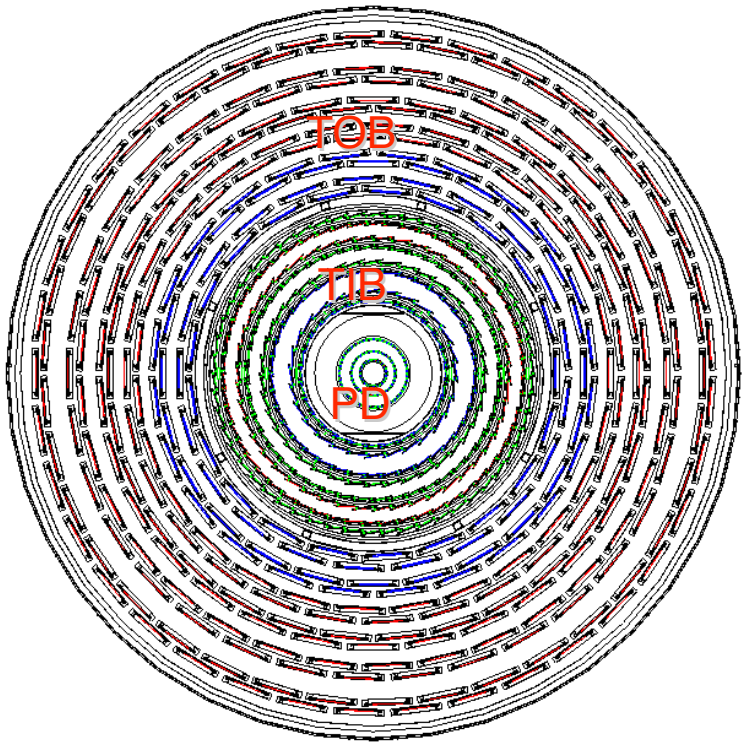
CMS Tracker General Structure

- Two main sub-systems: Silicon Strip Tracker and Pixel Detector
  - ~24m^3 SST ~ 240m^2 silicon P ~ 50kW
- Silicon Strip Tracker comprises 3 sub-detectors
  - Outer Barrel (TOB)
  - Inner Barrel and Disks (TIB-TID)
  - End-Cap (TEC)

Radiation environment
~10Mrad ionising
~10^{14} hadrons.cm^{-2}

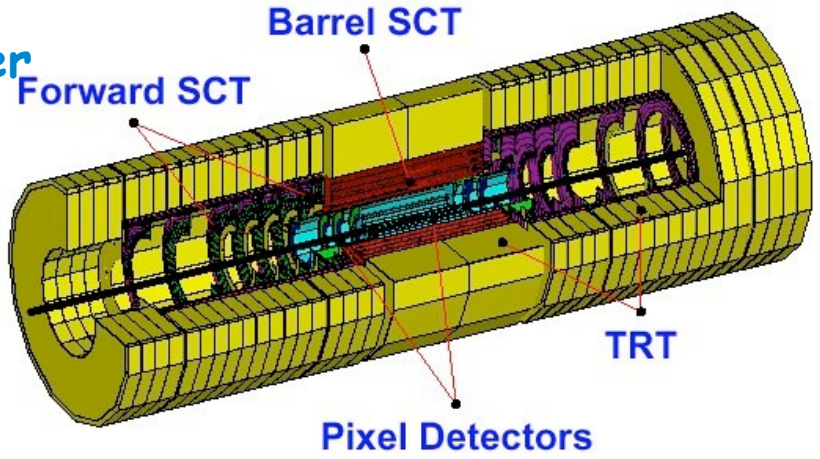
T ~ -20°C

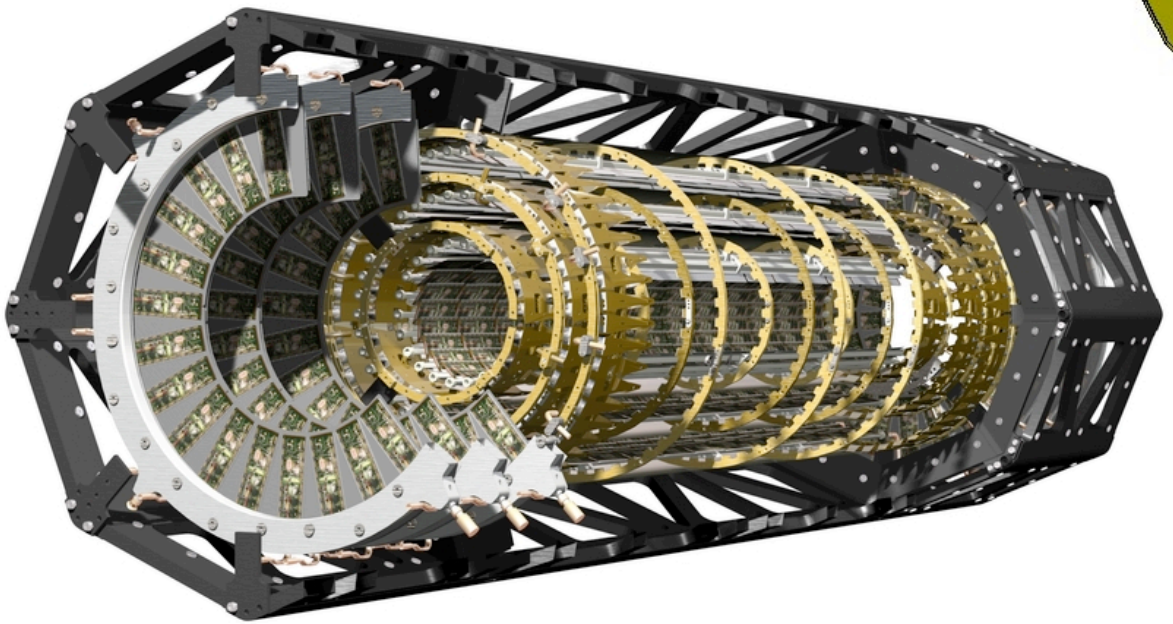




ATLAS Tracker Layout

- Sub-systems in 2T magnetic field
  - Straw Tube Transition Radiation Tracker 370k channels
  - SemiConductor Tracker 6M channels
  - Pixel Detector 80M channels



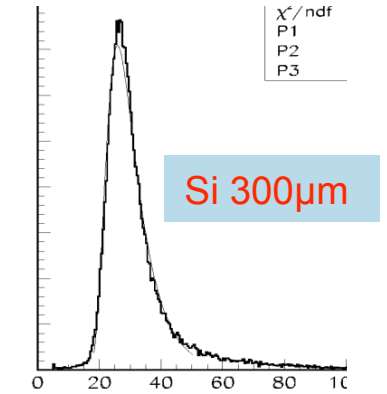


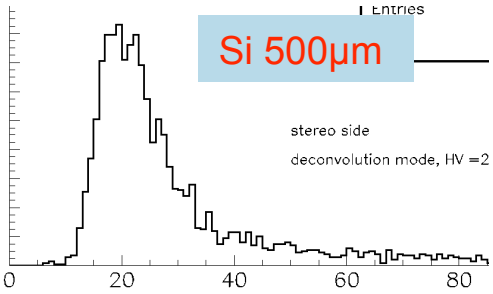
- Pixels:
  - 50μm x 400μm
  - 1.4m long x 0.5m diam
  - 2880 pixels/FE chip
  - 16 chips/module
  - Sensors 16mm x 60mm
  - 0.8W/cm^2 ->15kW

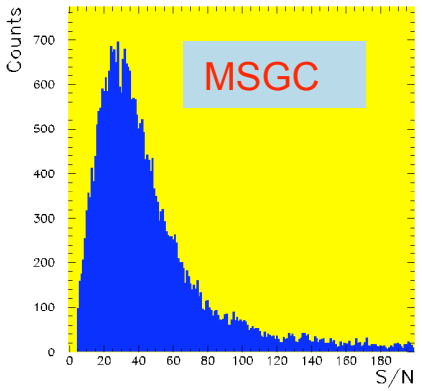
Tracker electronic requirements

physics	technical
high spatial precision	front-end circuit must be ASIC
large channel count	low power ~ mW/channel
limited energy precision	range of signals can be large
efficiency	good signal to noise for small signals
moderate linearity	to few MIPs
limited dynamic range	digitise ~6-8bits, or less!
long term performance	stability and no degradation
radiation tolerance	LHC radiation levels ~10Mrad but elsewhere often 0.3 - few Mrad Possible beam accidents cannot be ignored for tracking systems

1 Gray = 100 rads

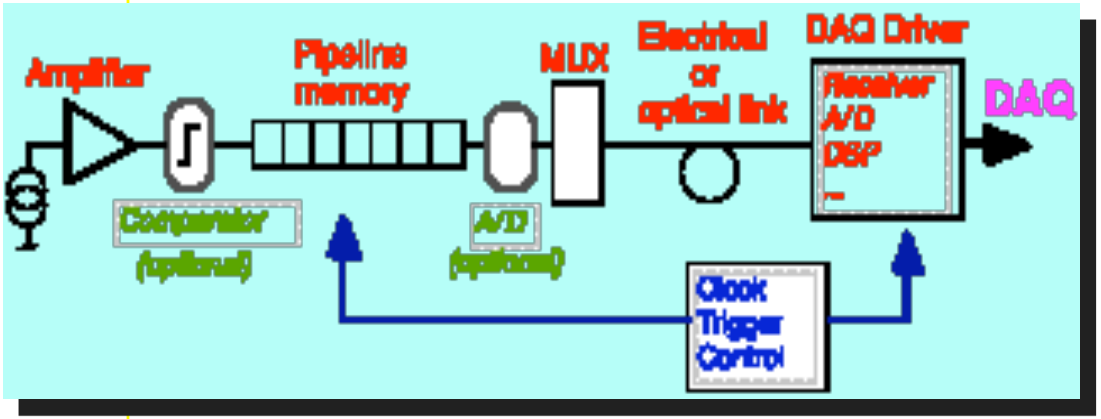


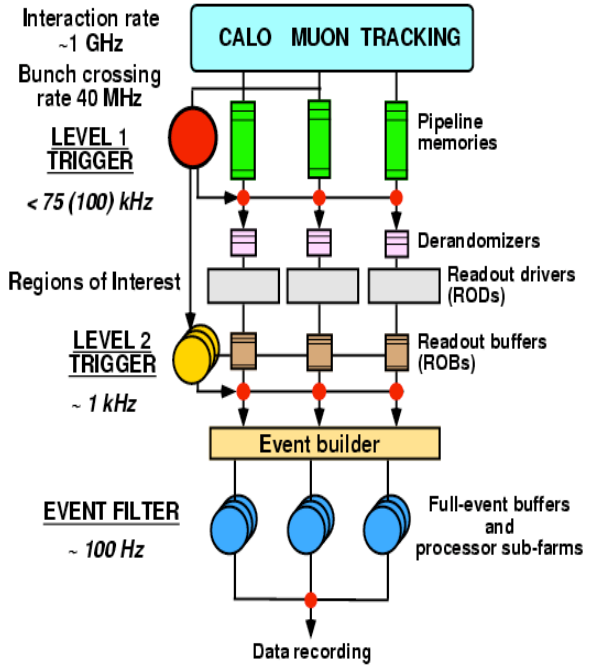




Generic (LHC) systems

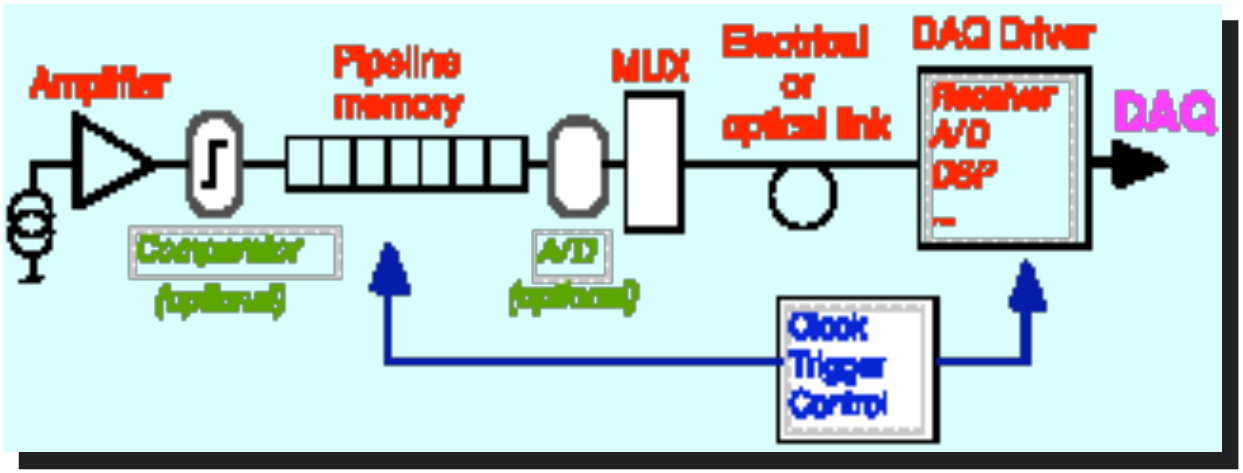
- functions required by all systems
  - amplification and filtering
  - analogue to digital conversion
  - association to beam crossing
  - storage prior to trigger (~ few μs)
  - (deadtime free readout @ ~100kHz)
  - storage pre-DAQ (~ms)
  - clock and trigger distribution
  - calibration
  - control
  - Monitoring
- Tracking systems do not usually contribute to first level triggers but
  - often desirable
  - depends on system latency

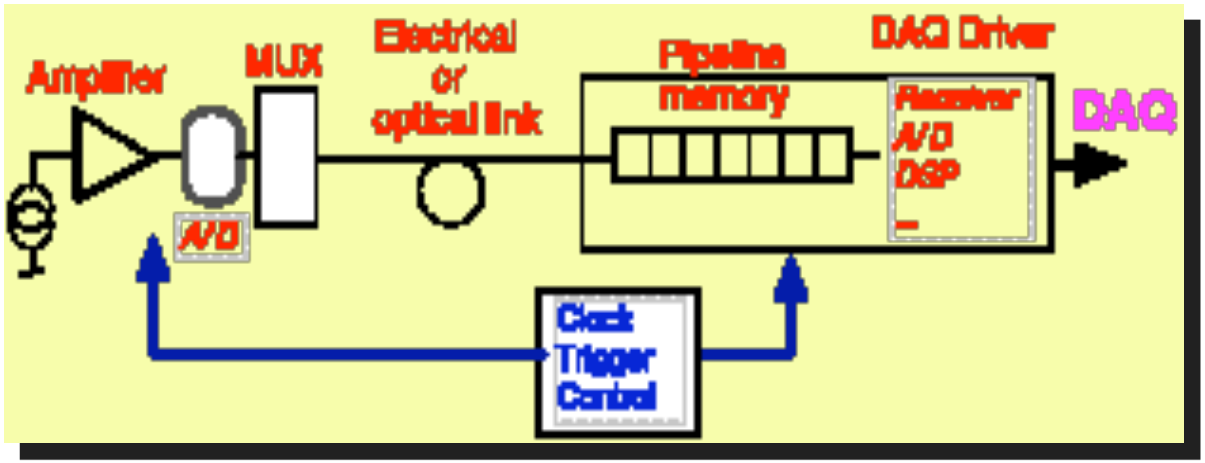




Possible implementations

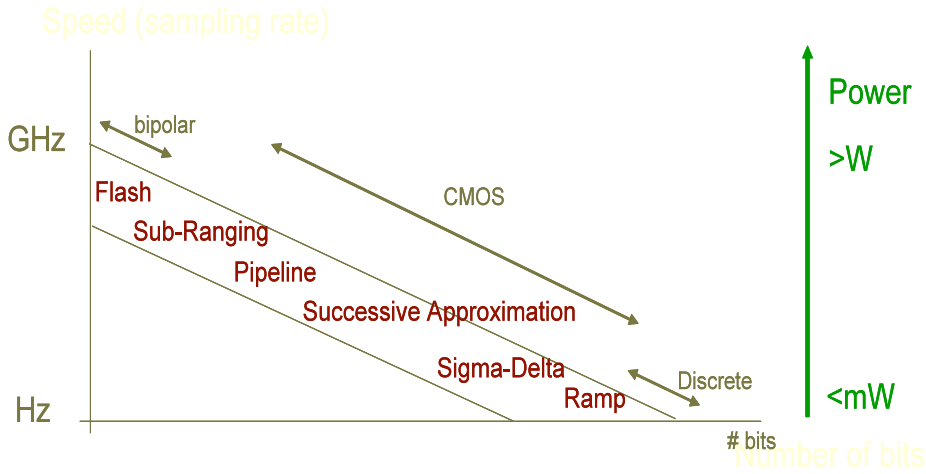
- There are usually several ways of doing the same thing
  - Ideally, take a system view from early design stage
  - Typical issues…
- A-D conversion
  - On-detector = power, custom components,…
  - Off-detector = no of links, cost,..
- Link technology
  - Electrical: power, speed, noise issues,..
  - Optical: cost, technical challenges,…

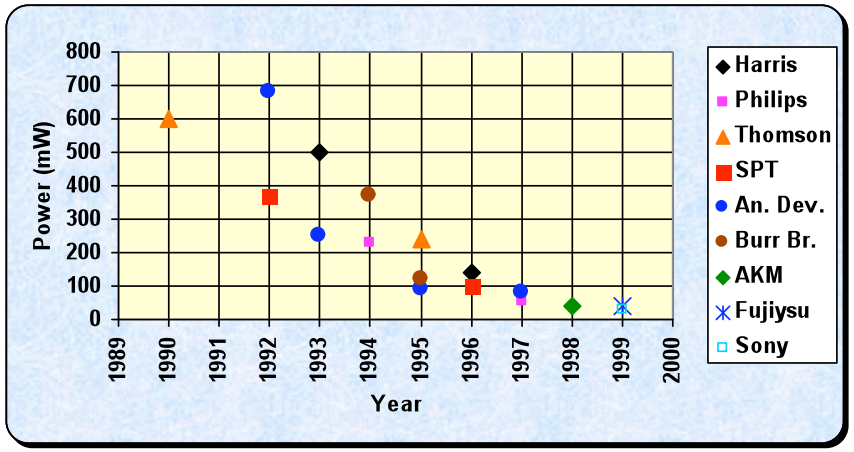




Analog to digital conversion

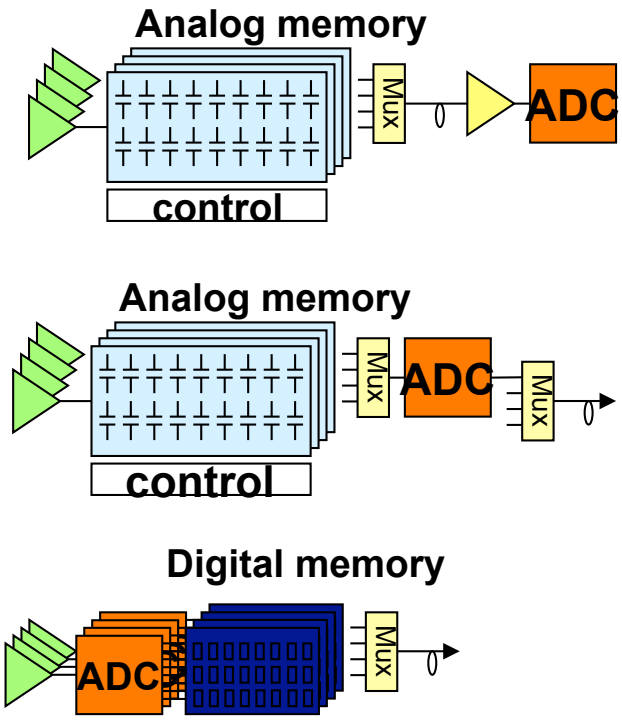
- There is clearly a tendency to go digital as early as possible
- The "cost" of the ADC determines which architecture is chosen
  - Strongly depends on speed and resolution
- Cost is here
  - Power consumption
  - Silicon area
  - Availability of radiation hard ADC
- High resolution ADC also needs low jitter clock to maintain effective resolution





Analog/Digital/Binary

- After proper amplification and shaping the signals must at some point be converted into the digital domain to allow final readout to DAQ system
- Analog readout
  - Analog buffering with digitization done after buffer or after analog transmission off detector (at DAQ interface)
- Analog buffer with digital readout
- Digital readout
  - Information digitized after shaping and all further processing done digital
- Binary: discriminator right after shaping
  - Binary tracking
  - Drift time measurement with following TDC

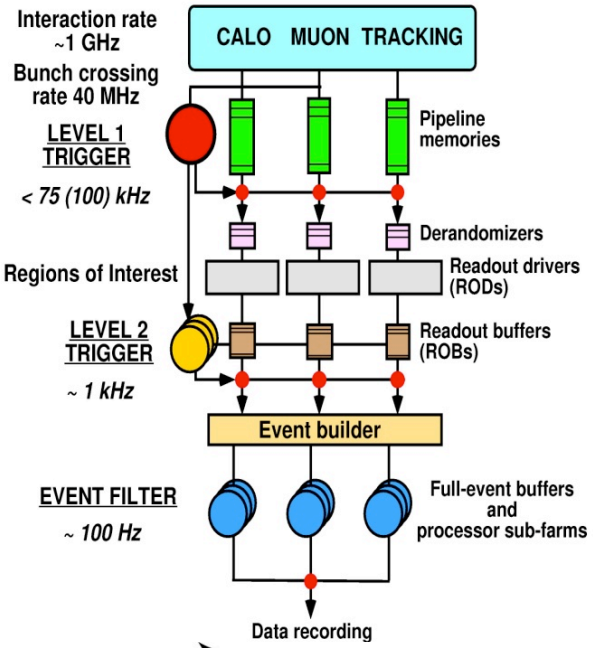


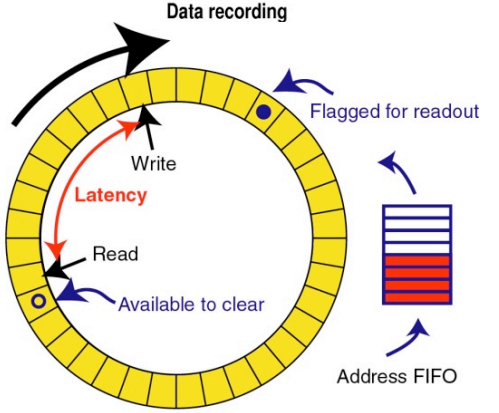
analogue vs digital

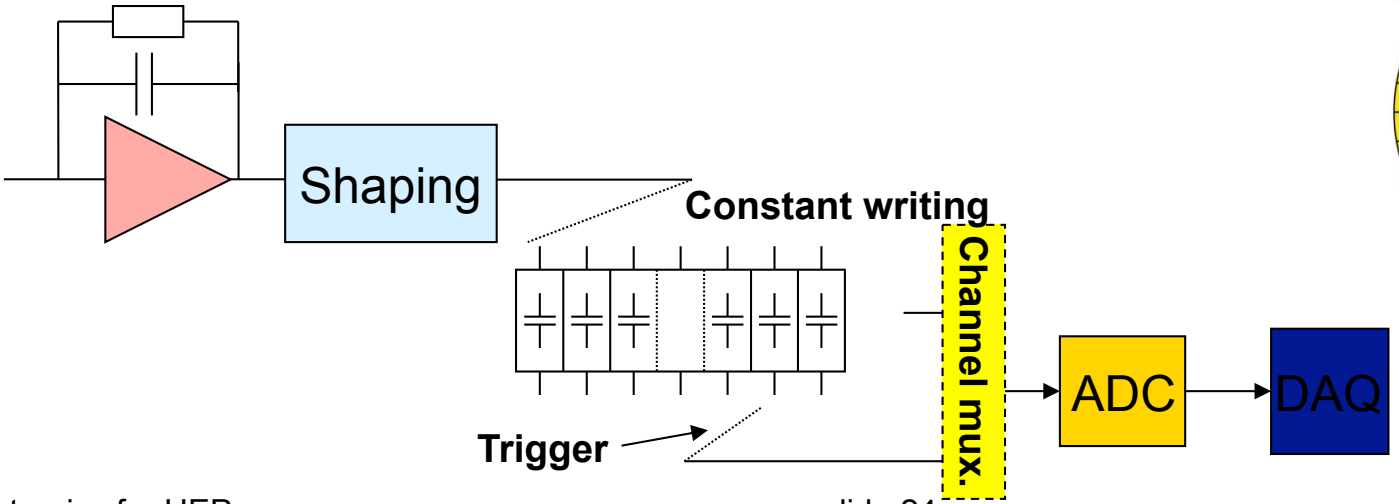
- Technology has been steadily moving digital for many years
  - Yet analogue tracker information widely valued. Why?
    - possible robustness against unexpected noise
    - ability to monitor data and detector quality easily
    - potential improved position resolution from charge sharing
    - power requirements and speed constraints, etc…
  - However,
    - possible noise and power issues for electrical analogue data transfer
    - commercial optical links are mostly digital
    - zero-suppression on-detector reduces data volume for transmission
    - binary is simplest system, etc…
  - But…
- Conclusion
  - No simple answer. Need careful comparison of alternative systems to make judgement, which depend on constraints
    - HEP experiments contain examples of most possible variants

Triggered

- Separate trigger system quickly determines events of interest and informs front-end about this
- Trigger processing requires some data transmission and processing time to make decision so front-ends must buffer data during this latency
- For constant high rate experiments a "pipeline" buffer is needed in all front-end detector channels: analog or digital
  1. Real clocked pipeline (high power, large area, bad for analog)
  2. Circular buffer
  3. Time tagged (zero suppressed latency buffer based on time information)
- Specific complications for detectors where more data samples must be extracted than minimum spacing between triggers (drift tubes).

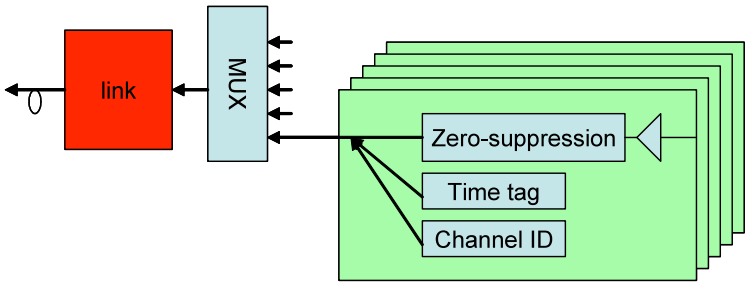


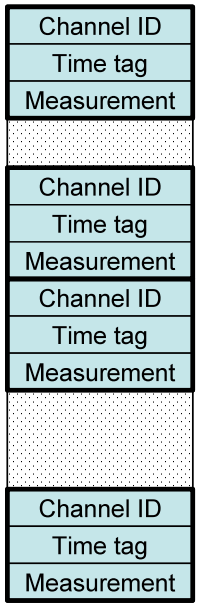




Local zero-suppression

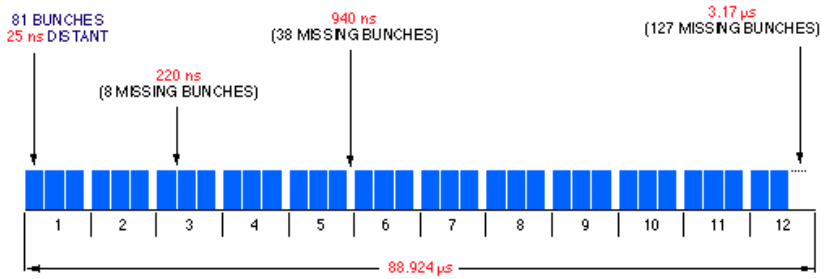
- Why spend bandwidth sending data that is zero for the majority of the time ?
- Perform zero-suppression on detector and only send data with real content
  - We do not want to loose information of interest so this must be done with great care taking into account pedestals, baseline variations, common mode, noise, etc.
  - Use of digital signal processing
  - Not worth it for occupancies above ~10%
- Gives some system problems that makes it non trivial
  - Data rates fluctuates all the time and we have to fit this into links with a given bandwidth
  - Not any more event synchronous
  - Complicated buffer handling (overflows)
  - Before an experiment is built and running it is very difficult to give reliable estimates of data rates needed (background, new physics, etc.)

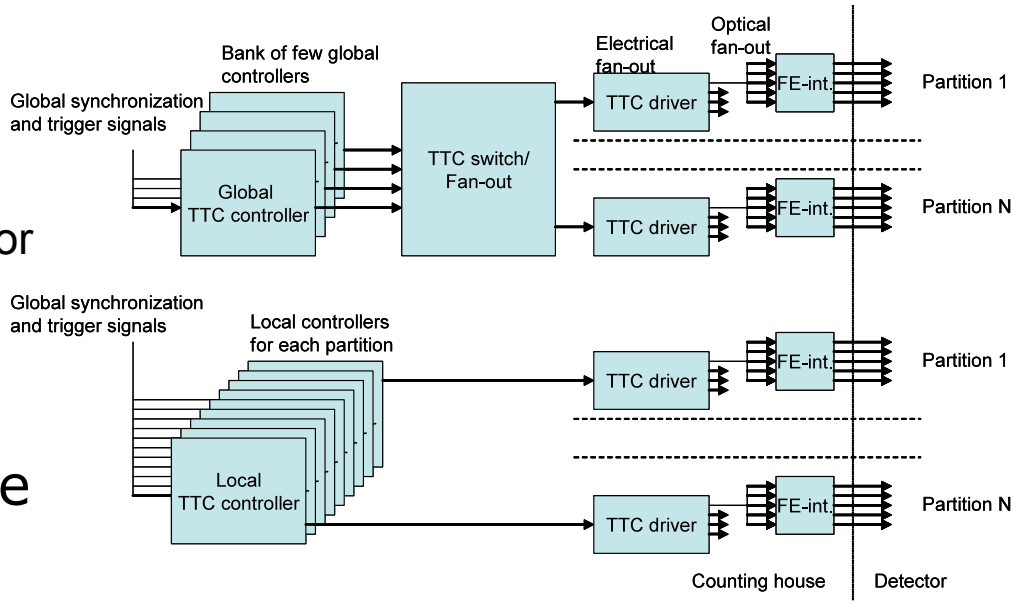




Timing & sync control

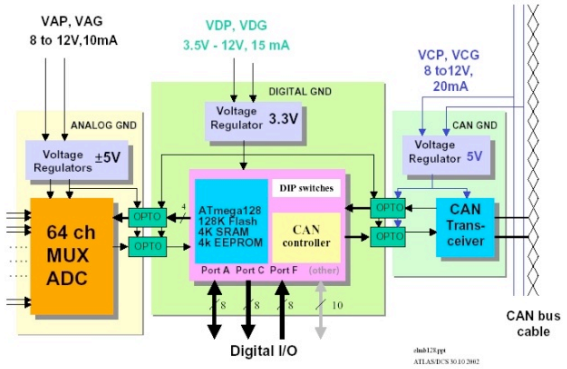
- Sampling clock with low jitter
- Synch reset
- Synchronization with machine bunch structure
- Calibration
- Trigger (with event type)
- Time align all the different sub-detectors and channels
  - Programmable delays
- Fan-out – unidirectional
  - Global fan-out to whole experiment or
  - Sub-detector fan-out
- Must be reliable as system otherwise may get de-synchronized which may take quite some time to correct

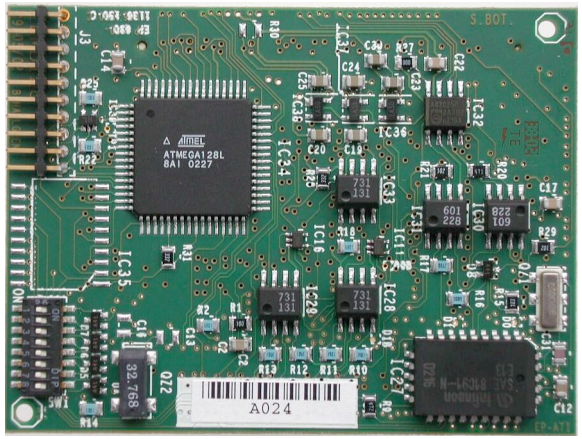




Control and monitoring

- Access to setup registers (must have read-back)
- Access to local monitoring functions
  - Temperatures, power supply levels, errors, etc.
- Bidirectional with addressing capability (module, chip, register)
- Speed not critical and does not need to be synchronous
  - Low speed serial bus: I^2C, JTAG, SPI
- Must be reasonably reliable (read-back to check correct download and re-write when needed)





Example: ELMB

Choice of ASIC technology

Technologies available

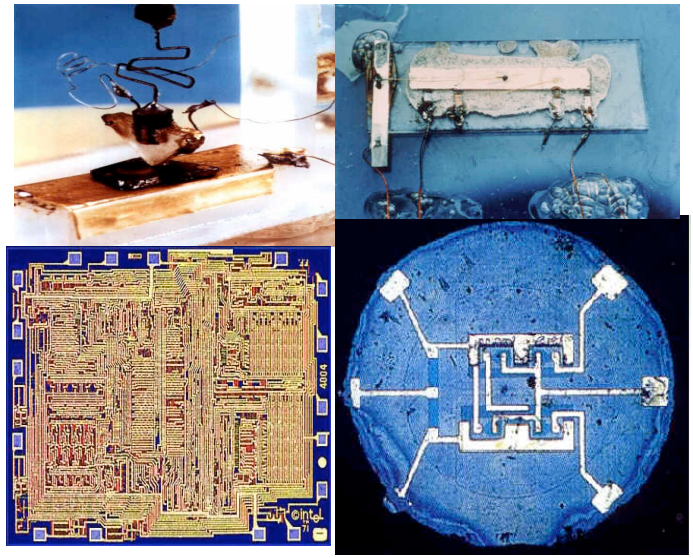
- Radiation tolerance has been a primary consideration for LHC
  - but a wide range of technologies can be accessed, often at low cost
- Standard CMOS - dominates
- Hardened CMOS
  - originally developed for military and space, in 1960s, most to ~1Mrad
  - few specialised processes, even fewer foundry services
  - expensive and not the most up-to-date feature size, eg. ~0.8µm
- bipolar - neutron sensitive, especially power devices
- GaAs - intrinsically hard to high level
  - few processes, not analogue
- SoI/SOS CMOS (Silicon on Insulator, Silicon on Sapphire)
  - investigated but excessive noise

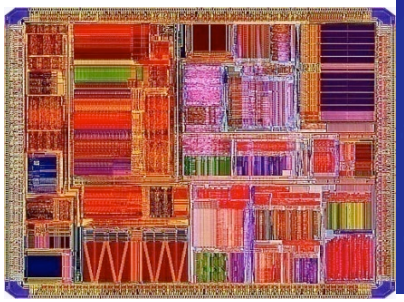
CMOS technology

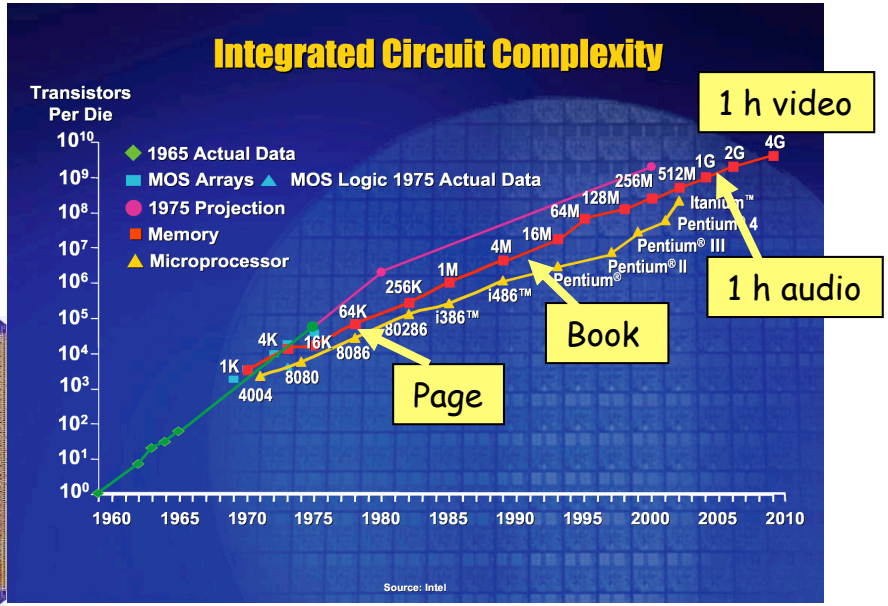
- Standard commercial CMOS has become the preferred technology
  - partly because of accessibility…
- Commercial electronics is dominated by CMOS
  - It is very costly to swim against the stream
  - HEP is a very small community compared to industry
    - Largest LHC orders <1000 wafers
    - Commercial foundry production >40,000 wafers per month
  - There are benefits from adopting a few common technologies and standards
- Modern CMOS meets speed and power constraints
  - Smallest feature size in common use 0.25µm - but industry at ~0.09µm
  - Coarser feature sizes still available and in use (eg. 0.35-1µm)
- It has been shown to be very radiation hard
  - But has advantages in all ASIC developments
  - Quality and uniformity have been demonstrated to be high

IC technologies

- The fast development of IC technologies is what has enabled current detectors with their electronics to be built
- It has been our luck that the 0.25um CMOS technology can be used in very high radiation environments (with appropriate special design techniques).
  - The following 0.18um and 0.13um is even better
- Next generation technologies are much more complicated and very expensive (~1M$ for masks) so we may have to rethink how our community makes chips for HEP.
- The close integration of integrated circuits and detectors are critical: Combined electronics and detectors and 3D packaging will pose new challenges.



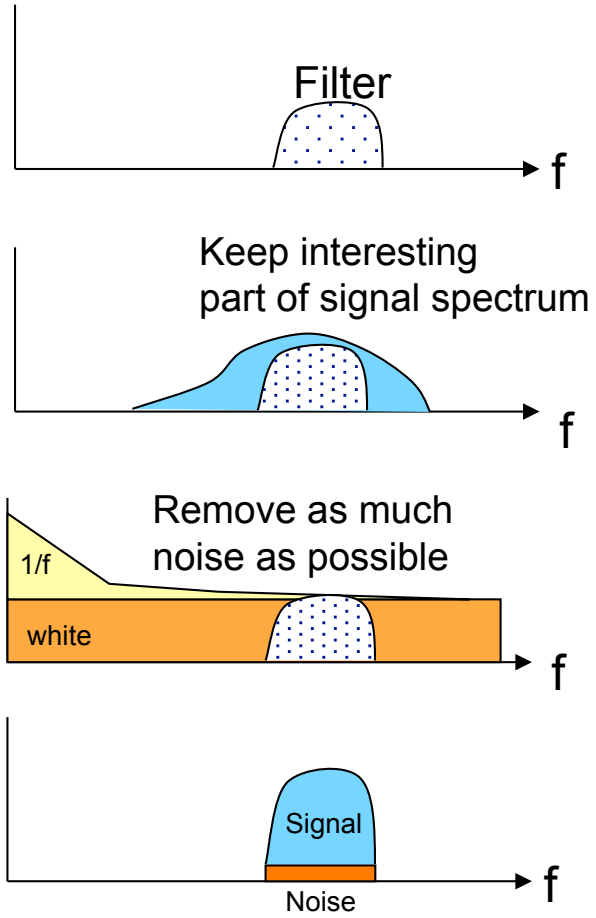




Signal/Noise Ratio

Signal & Noise filtering

- The total noise will depend on the effective bandwidth of the circuit
  - Shaping/filtering
- Minimize bandwidth to what is really needed
  - Worth to sacrifice a part of the signal to decrease noise
  - What counts is Signal/Noise Ratio (SNR)
- Determined by bandwidth of interest in detector signal
  - Speed of detector itself
  - Time separation of hits from consecutive collisions
  - Need for time information (e.g. drift time)

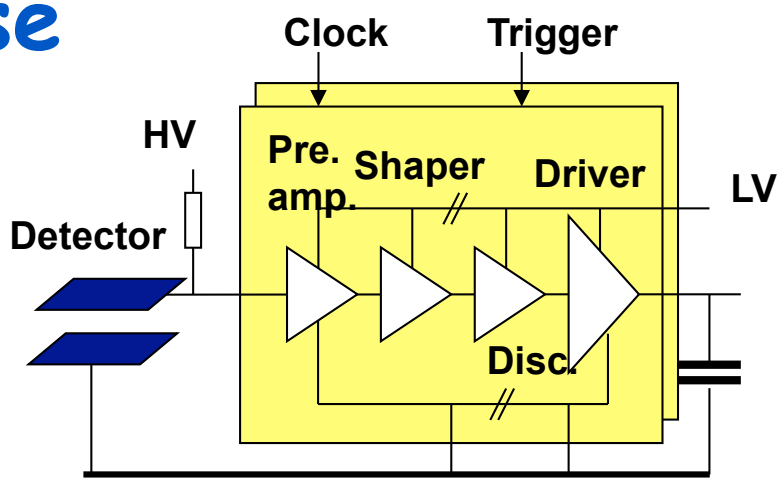


Minimizing crosstalk

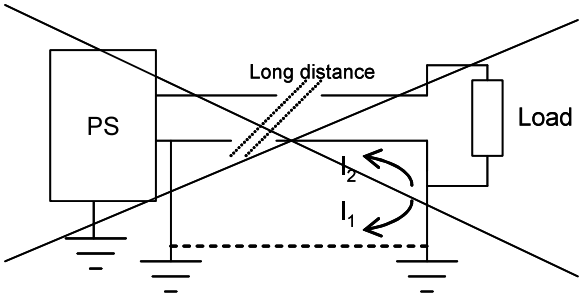
- Crosstalk effects increasingly important as channel densities in modern detectors constantly increasing.
  - In fine grain pixel detectors capacitance to neighbor pixels gives a significant contribution

Minimizing system noise

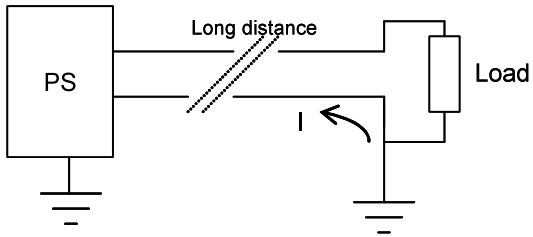
- Critical coupling between detector and its electronics.
  - Typical problem of coupling from outputs of FE chips to the very sensitive inputs: Oscillators are not so difficult to make !.



- Power supply noise
  - Analog FE can be very sensitive to any power supply noise
  - Use of floating power supplies to prevent forcing high return currents into global grounding of experiment and its electronics
  - Often a general confusion about power return and ground



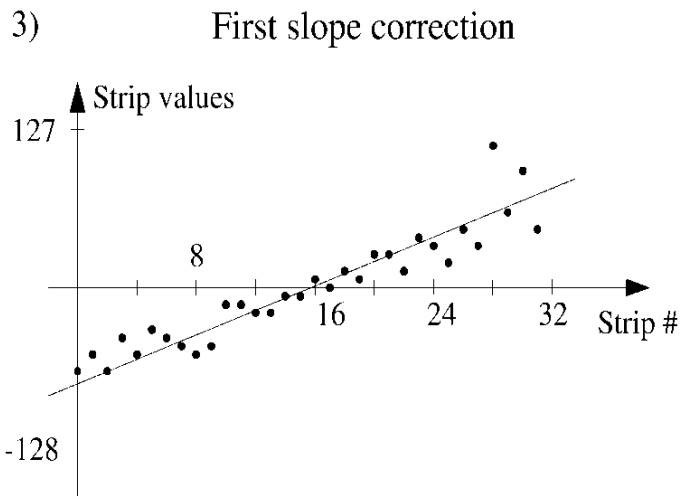
Generation of return currents in grounding network

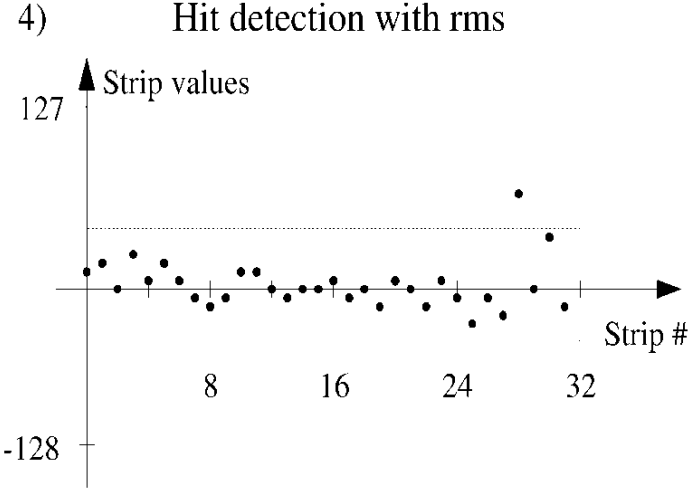


No return currents in grounding network

Common mode suppression

- Suppression of systematic noise sources from a non perfect system
- Fixed pedestal or dynamic pedestal per channel
- Systematic effect across channels in same event
  - Typically per front-end chip or front-end module
- The "shape" of the systematic effect must be known in advance
  - Proportional to detector capacitance (if varying across channels)
  - Proportional to distance to a given noise source (beam for a vertex detector)
- Channels with active hits must somehow be exclude from the calculation of the common mode
  - Iterative processing with simple thresholding
- This only works if one has access to full analog information from all channels in same event
  - Must be done before zero-suppression is performed

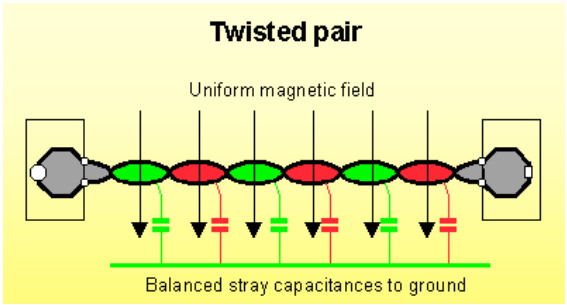


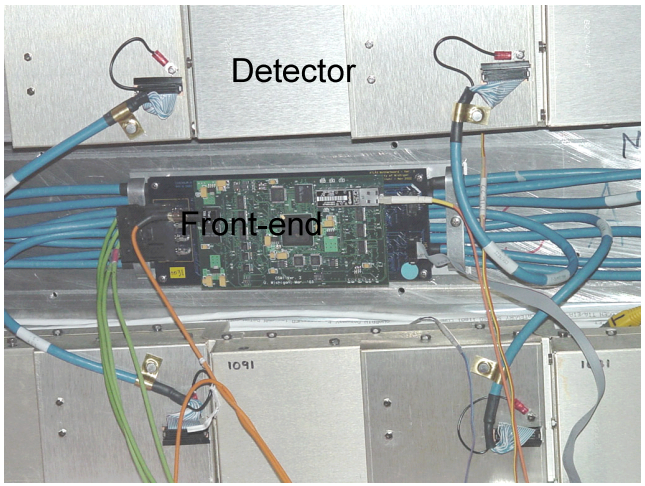


And then do it again with detected hits removed from common mode calculation

EMC (Electromagnetic Compatibility)

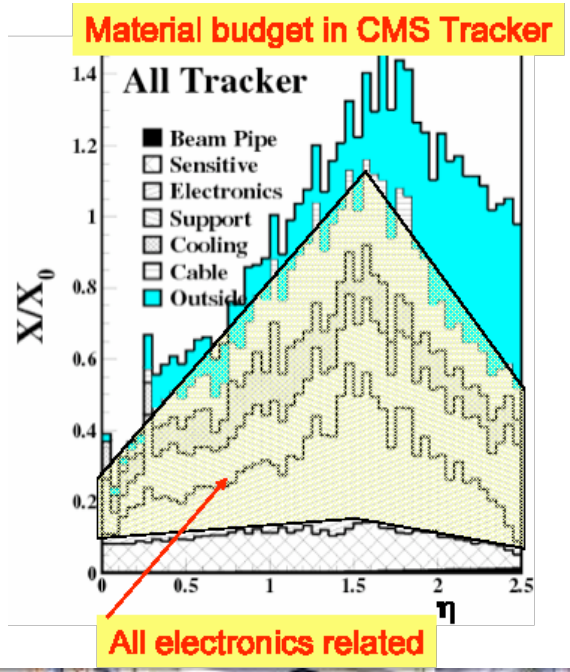
- **Shielding-Grounding-EMC**
  - This is a critical and far from easy aspect of large scale systems
  - Faraday cage shielding of whole detector and front-end electronics.
  - Use of differential and optical signals when ever possible
  - Twisted pairs when ever possible to minimize noise pickup and noise generation (also for power)
  - Grounding non trivial and there are different "religions"

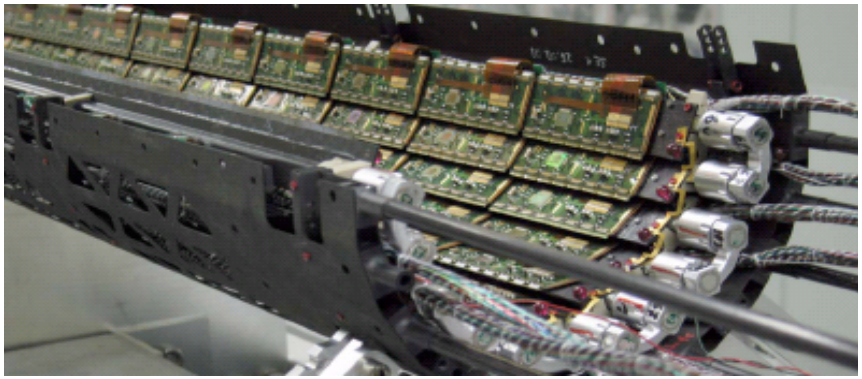


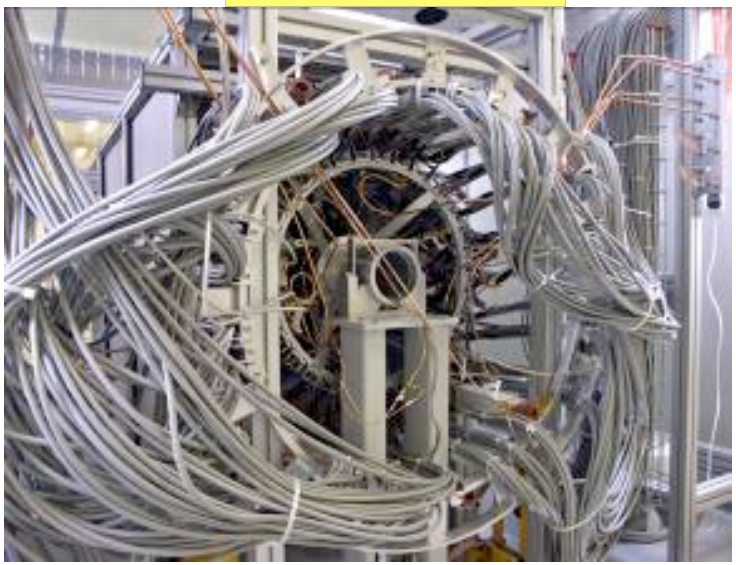


Powering

- Delivering power to the front-end electronics highly embedded in the detectors has been seen to be a major challenge (underestimated).
- The related cooling and power cabling infrastructure is a serious problem of the inner trackers as any additional material seriously degrades the physics performance of the whole experiment.
- A large majority of the material in these detectors in LHC relates to the electronics, cooling and power and not to the silicon detector them selves (which was the initial belief)
- How to improve
  1. Lower power consumption
  2. Improve power distribution

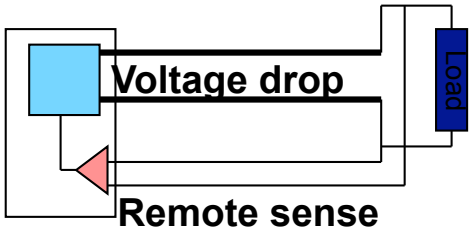


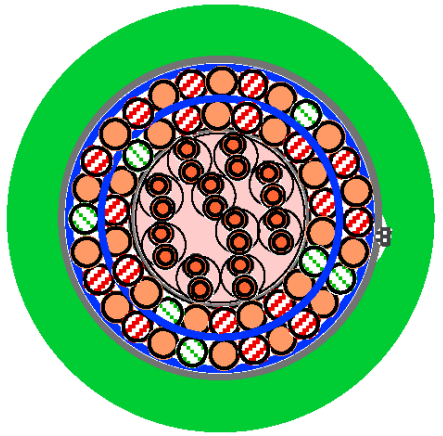


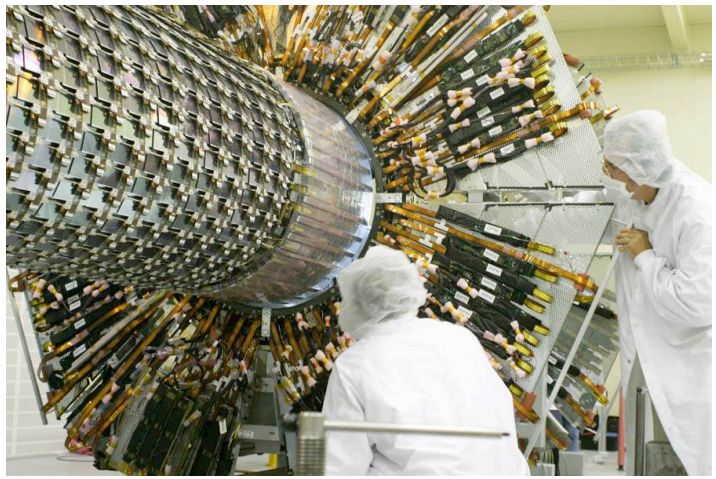


The problem as is

- Total power: ~500kw (to be supplied and cooled)
  - Trackers: ~ 60 kW
  - Calorimeters: ~ 300 kW
  - Muon: ~ 200 kW
  - Must for large scale detectors be delivered over 50m – 100m distance
- Direct supply of LV power from ~50m away
  - Big fat copper cables needed
    - Use aluminum cables for last 5-10m to reduce material budget
  - Power supply quality at end will not be good with varying power consumption (just simple resistive losses)
    - If power consumption constant then this could be OK
  - Use remote sense to compensate
    - This will have limited reaction speed
    - May even become unstable for certain load configurations
  - Power loss in cables will be significant for the voltages (2.5v) and currents needed: ~50% loss in cables (that needs to be cooled)
- Use of local linear regulators
  - Improves power quality at end load.
  - Adds additional power loss: 1 – 2 v head room needed for regulator
  - Increases power losses and total efficiency now only: ~25% (more cooling needed)

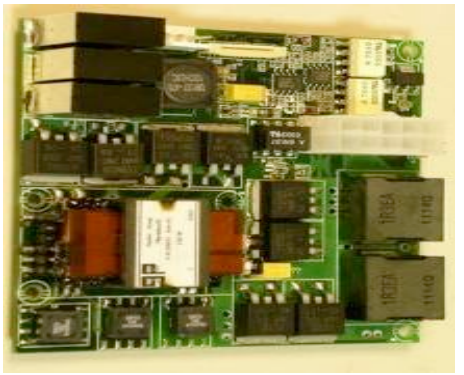






Use of DC-DC converters

- **For high power consumers (e.g. calorimeter) the use of local DC-DC converters are inevitable.**
- **These must work in radiation and high magnetic fields**
  - **This is not exactly what switched mode DC-DC converters like**
  - **Magnetic coils and transformers saturated**
  - **Power devices do not at all like radiation:**
    SEU - > single event burnout -> smoke -> disaster
- **DC-DC converters for moderate radiation and moderate magnetic fields have been developed and used**
  - **Some worries about the actual reliability of these for long term**

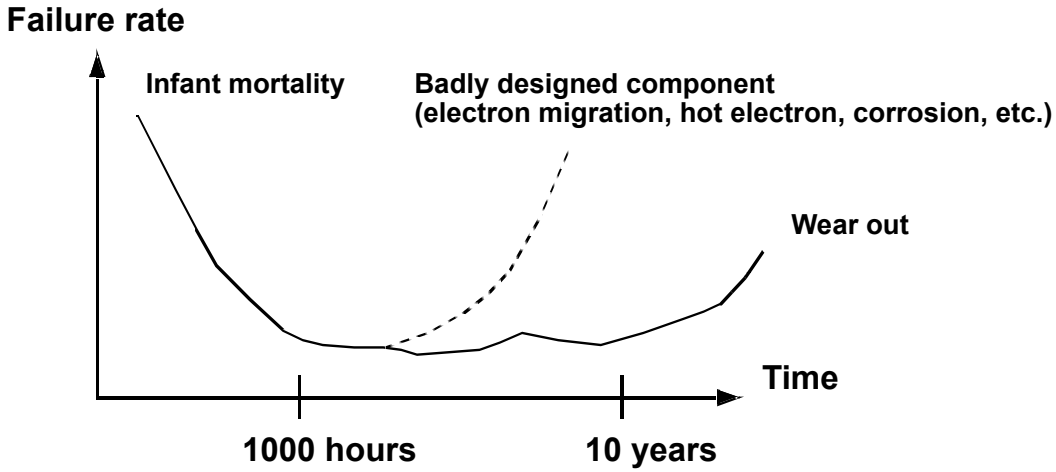


Low power

- Very low power designs are key for future tracker detectors
  - Willing to sacrifice other performance figures: resolution, etc.
- The largest part of the power is normally burned in the pre-amplifier where large transistors with a significant biasing current is used to get the lowest noise.
- What gives the least material tracker: ?
  - Thin silicon where the pre-amplifiers must be very low noise and therefore consumes quite some power
  - Thick silicon with lower power pre-amplifier
- Use of SiGe bipolar technology (very fast but expensive)
- Use of pulsed power in experiments with a spill structure (not LHC but ILC and CLIC)
  - All the analog biasing circuits must then be quick to stabilize
  - Large current variations in cables, connectors and bond wires that will then tend to move/oscillate when in a strong magnetic field and may then break (this problem has been seen in the past)
  - Thermal effects as not running with constant power.

Reliability

- Front-end electronics are in many cases enclosed in locations where it is very difficult to replace or repair it.
- Harsh environment (radiation ,magnetic fields, cooling, etc.)
- Huge systems (so there will always be something not working)
  - Detector layout has in most cases been made such that a failing module in a detection layer does not significantly deteriorate physics performance
  - Calorimeter is only single layer !
- Electronics will not work for ever
- Most failures occur in the beginning of its lifetime (infant mortalities)
- Infant mortalities can be sorted out by burn-in
  - Run electronics at increased temperature (or even better with temperature cycling) for 24hours or more
- All electronics located within detector with difficult access must pass serious reliability qualification.
- In some cases special redundancy must be implemented



Failing parts within first 1000 hours: ~0.1%

Radiation effects

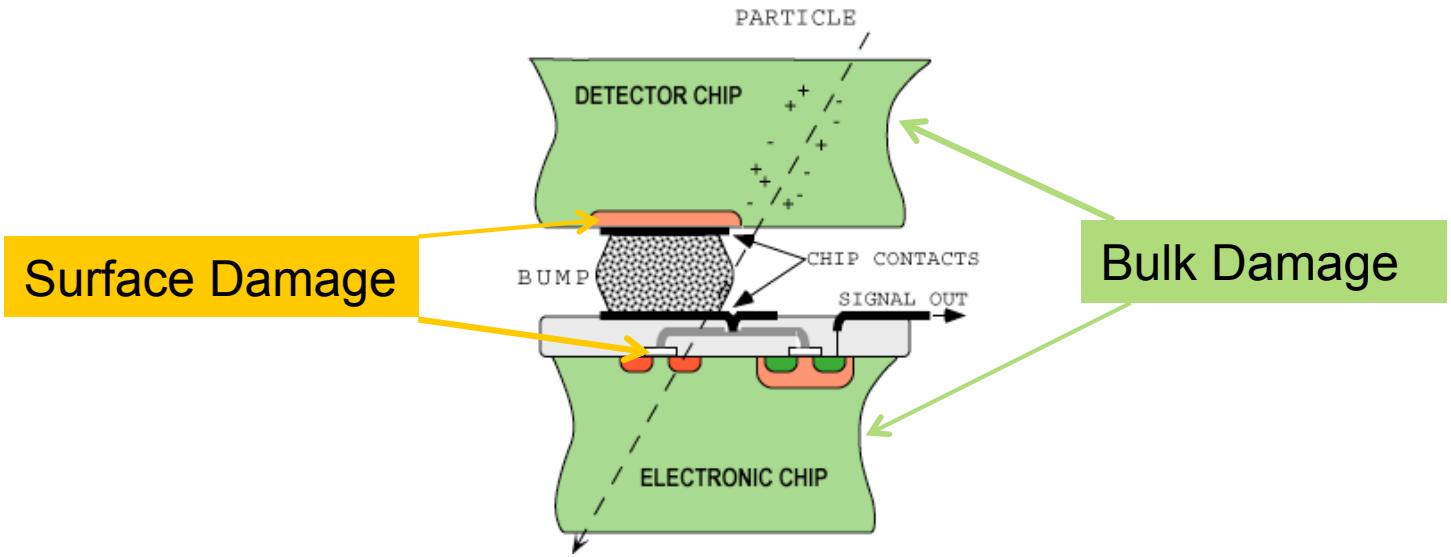
Radiation effects

- In modern experiments large amounts of electronics are located inside the detector where there may be a high level of radiation
  - This is the case for 3 of the 4 LHC experiments (10 years running)
    - Pixel detectors: 10 -100 Mrad
    - Trackers: ~10Mrad
    - Calorimeters: 0.1 – 1Mrad
    - Muon detectors: ~10krad
    - Cavern: 1 – 10krad
- Normal commercial electronics will not survive within this environment
  - One of the reasons why all the on-detector electronics in the LHC experiment are custom made
- Special technologies and dedicated design approaches are needed to make electronics last in this unfriendly environment
- Radiation effects on electronics can be divided into three major effects
  - Total dose (TID, Total Ionising Dose)
  - Displacement damage (NIEL, Non Ionising Energy Loss)
  - Single Event Effect (SEE, Effect of large ionising impact on critical nodes)
    - SEU : single event Upset = bit flip
    - SEL : single Event Latchup : destructive !

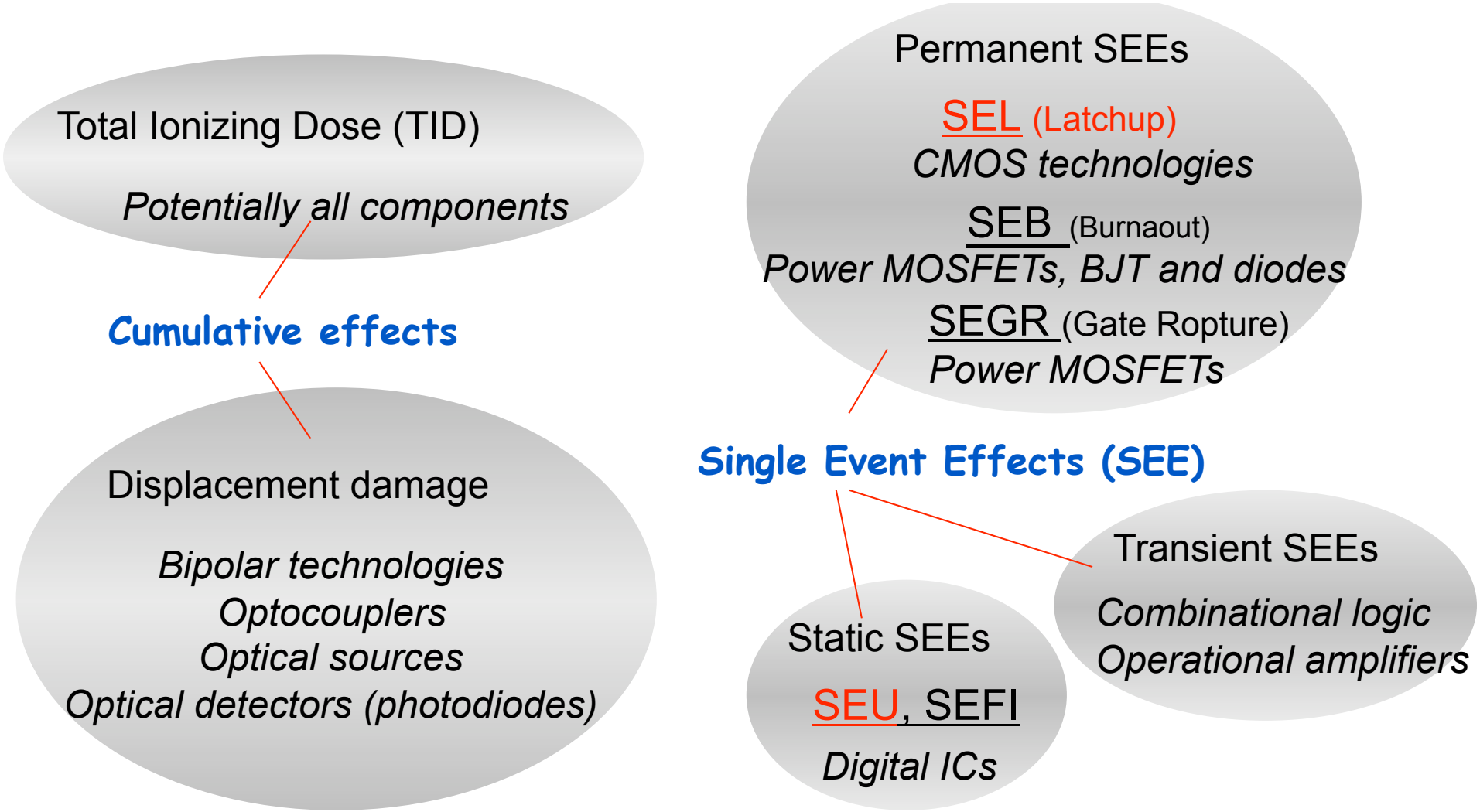
Radiation Environment in LHC Experiments

	TID (ionising dose)	Fluence 1MeV $n_{eq.}/cm^2$ in 10 years
ATLAS Pixels	50 Mrad	1.5×10^{15}
ATLAS Strips	7.9 Mrad	2×10^{14}
CMS Pixels	~24Mrad	$\sim 6 \times 10^{14}$
CMS Strips	7.5Mrad	1.6×10^{14}
ALICE Pixel	250krad	3×10^{12}

100 rads = 1 gray(Gy) = one joule of ionizing radiation absorbed by one Kilogram of matter

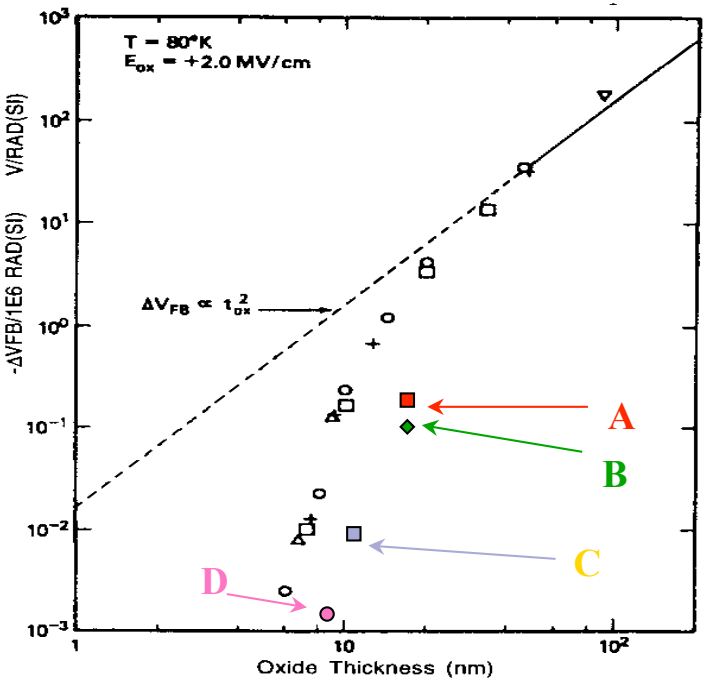


Summary of radiation effects



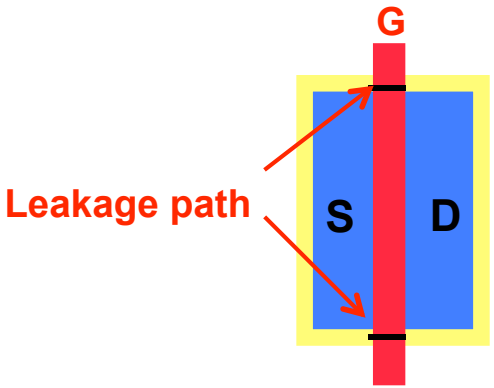
Total dose

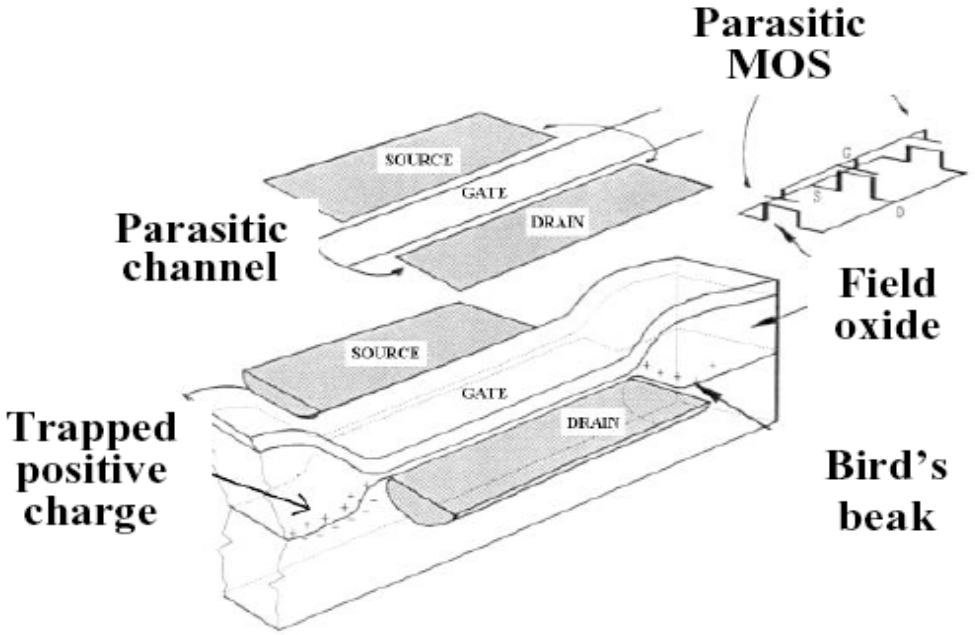
- Generated charges from traversing particles gets trapped within the insulators of the active devices and changes their behavior
- For CMOS devices this happens in the thin gate oxide layer which have a major impact on the function of the MOS transistor
  - Threshold shifts
  - Leakage current
- In deep submicron technologies (<0.25um) the trapped charges are removed by tunneling currents through the very thin gate oxide
    - Only limited threshold shifts
- The leakage currents caused by end effects of the linear transistor can be cured by using enclosed transistors
  - For CMOS technologies below the 130nm generation the use of enclosed NMOS devices does not seem necessary. But other effects may show up
- No major effect on high speed bipolar technologies



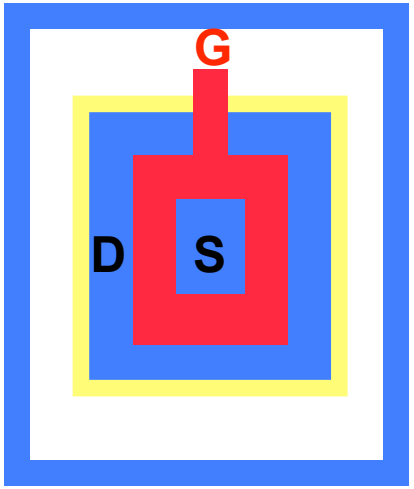
After N.S. Sacks, M.G. Ancona, and J.A. Modolo, IEEE Trans.Nucl.Sci., Vol.NS-31 (1984) 1249

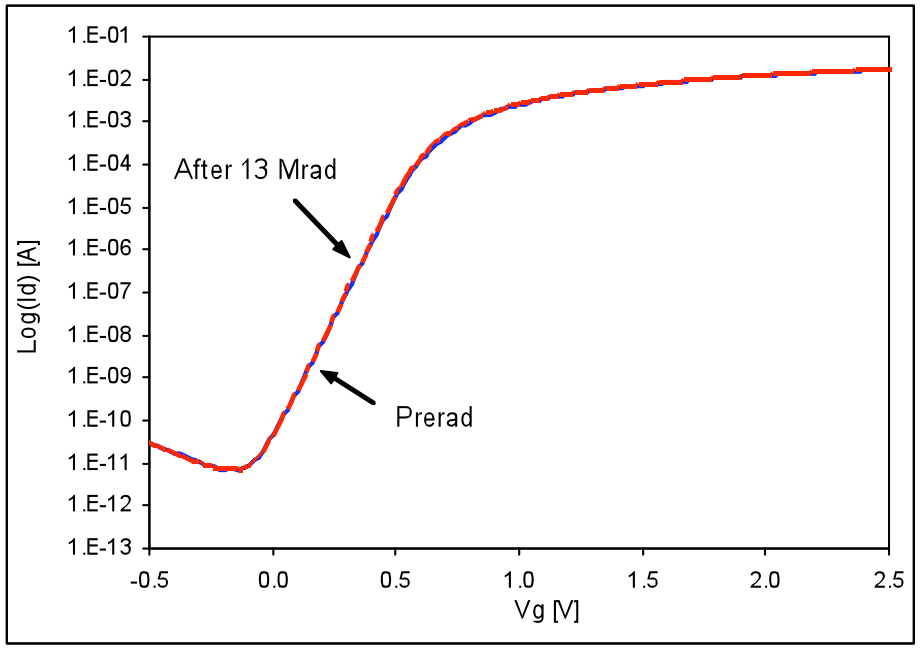
Radiation hardness by design



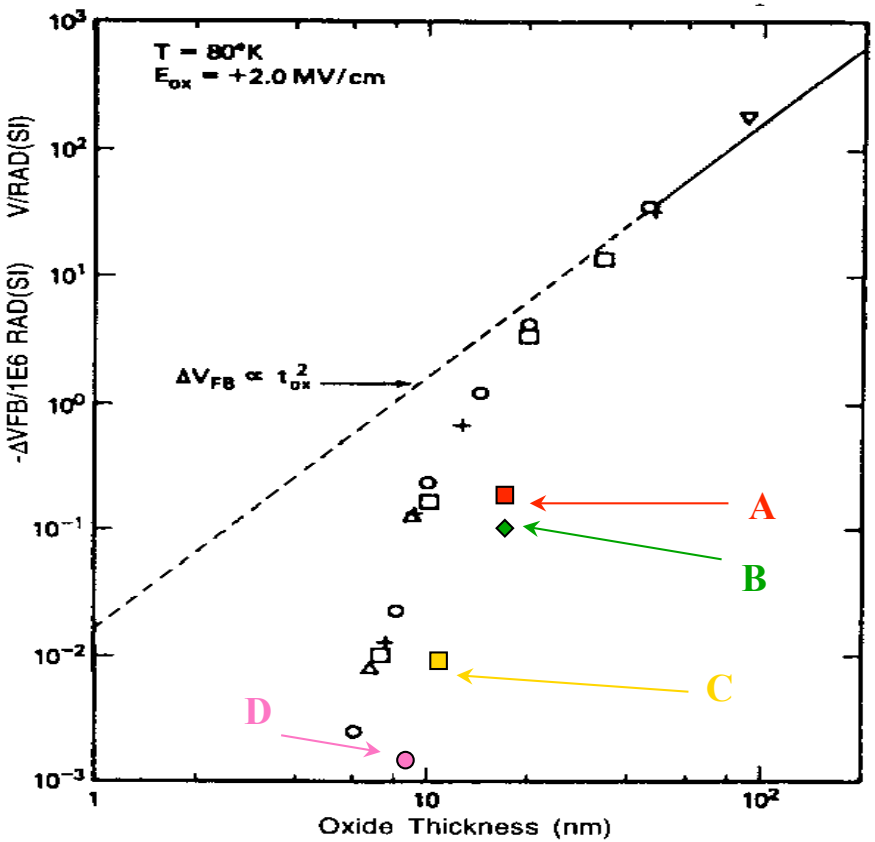


Enclosed layout transistors :
radtol up to > 13 Mrad in
0.25 µm standard CMOS (CERN)





Why DSM is so radiation tolerant



After N.S. Sacks, M.G. Ancona, and J.A. Modolo, IEEE Trans.Nucl.Sci., Vol.NS-31 (1984) 1249

- Gate oxide thickness scales with process feature size
  - simple arguments => $\Delta V \sim t_{ox}^2$
- Electron tunneling neutralizes trapped holes in thin oxides.
- Total dose effects, such as V_t shift, are naturally reduced in deep submicron processes.

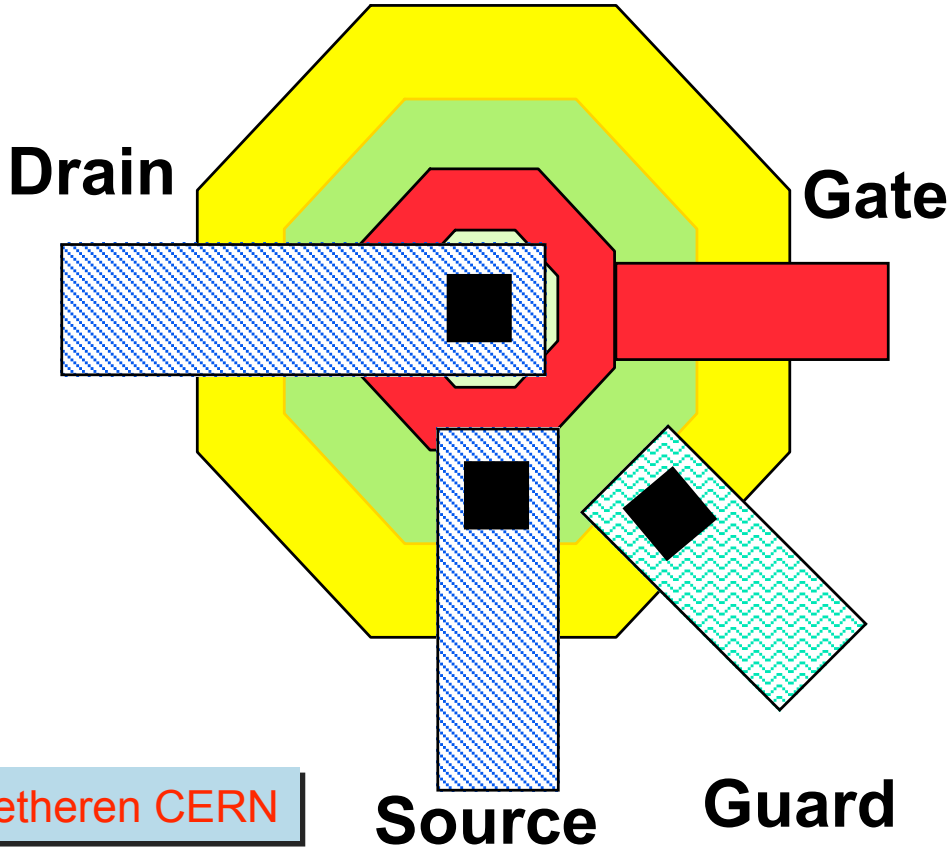
M. Letheren CERN

Radiation tolerant design

Thin gate-oxides + Gate all-around layout

- Min-size NMOS layout
  - Edge-less structure eliminates leakage via parasitic edge transistor.
  - Guard ring eliminates leakage between devices and provides latch-up protection.
  - Higher capacitance of gate all-around structure improves SEU tolerance.

    Further SEU tolerance by circuit design (SEU-tolerant flip-flops) or system design (triple-redundant logic, error detection and correction coding etc.)



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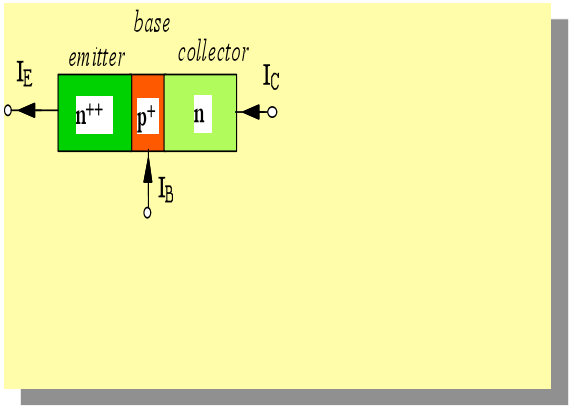
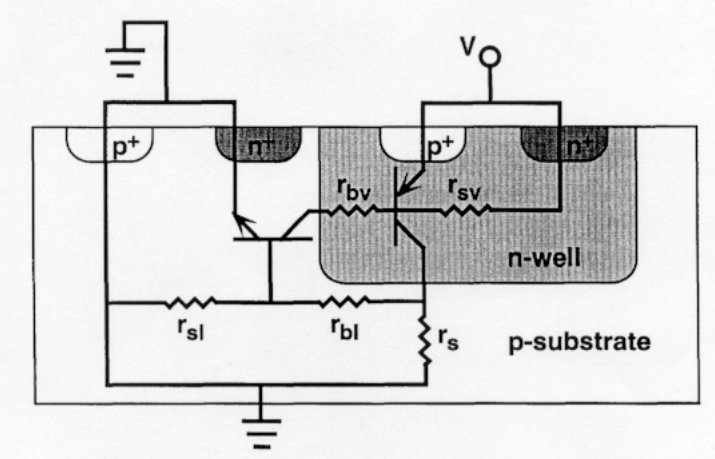
Displacement damage

- Traversing hadrons provokes displacements of atoms in the silicon lattice.
- Bipolar devices relies extensively on effects in the silicon lattice.
  - Traps (band gap energy levels)
  - Increased carrier recombination in base
- Results in decreased gain of bipolar devices with a dependency on the dose rate.
- No significant effect on MOS devices
- Also seriously affects Lasers and PIN diodes used for optical links.



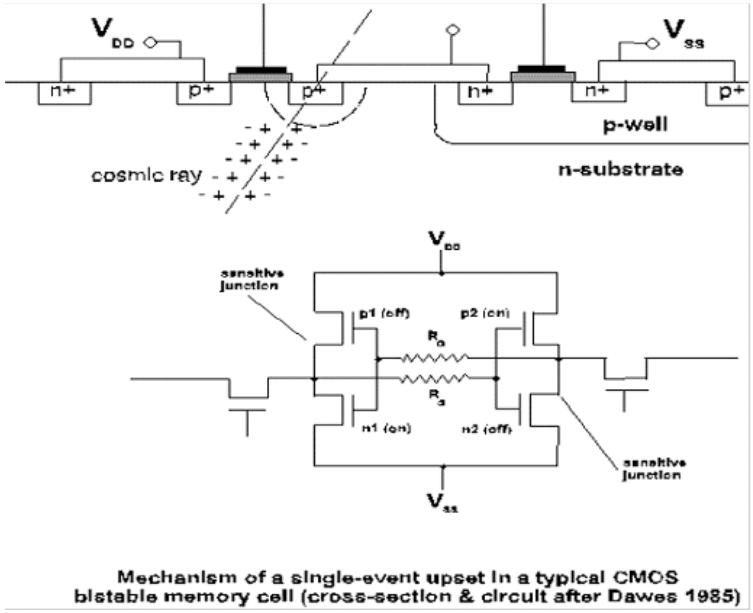
Single event latch-up

- Deposited charge from traversing particles provokes a power supply short circuit via an intrinsic parasitic device in CMOS technologies
- Traversing hadrons can only deposit sufficient charge if they make nuclear interaction with silicon
  - Heavily ionizing particles can generate the SEL directly
- The latchup circuit can by the IC technology be made such that it does not trigger.
- For modern technologies, with low power supply voltage, the latch-up can in general not be generated

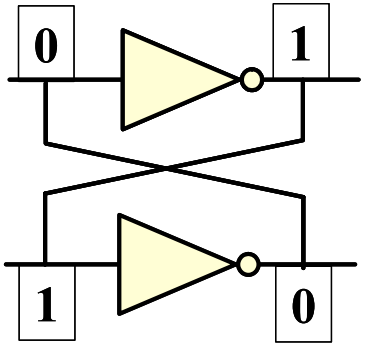


Single event upsets

- Deposition of sufficient charge can make a memory cell or a flip-flop change value
- As for SEL, sufficient charge can only be deposited via a nuclear interaction for traversing hadrons
- The sensitivity to this is expressed as an efficient cross section for this to occur
- This problem can be resolved at the circuit level or at the logic level
- Make memory element so large and slow that deposited charge not enough to flip bit
- Triple redundant (for registers)



Mechanism of a single-event upset in a typical CMOS bistable memory cell (cross-section & circuit after Dawes 1985)



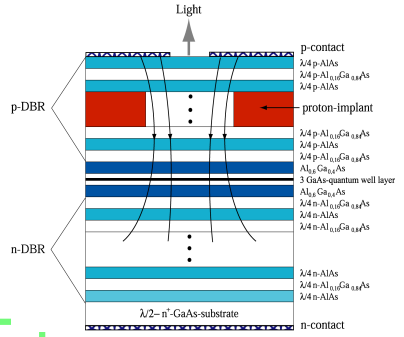
Use of COTS in radiation

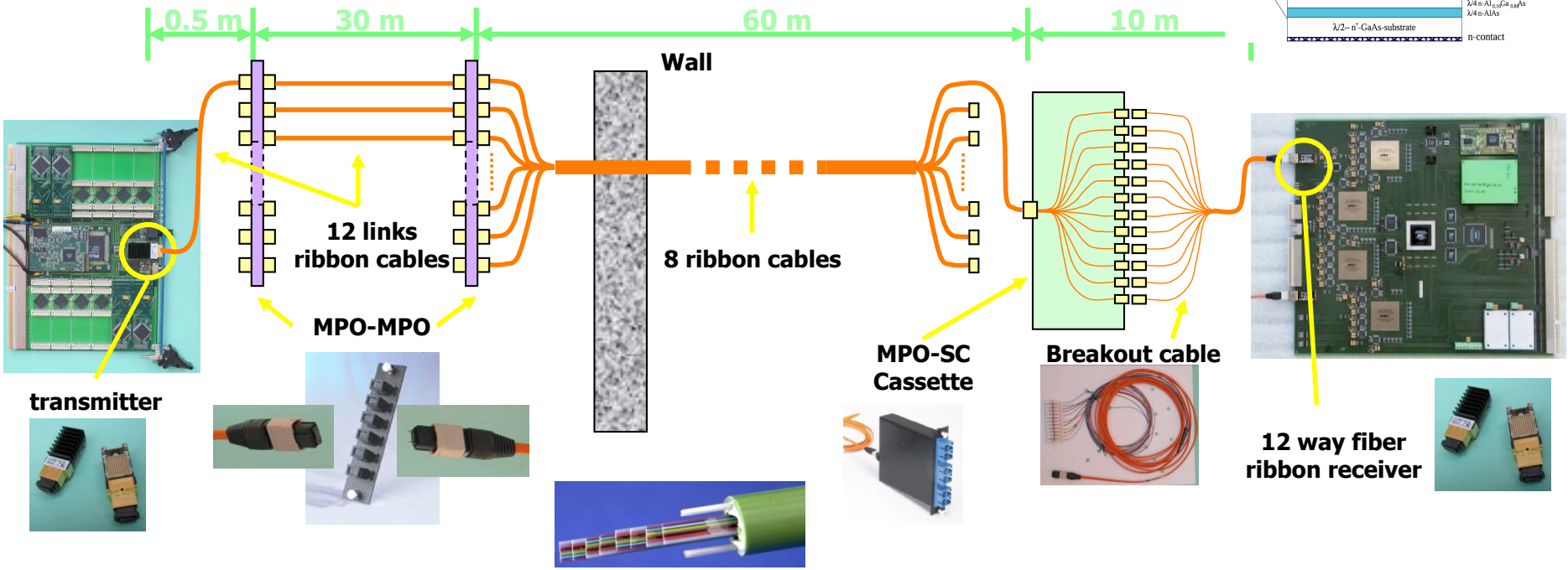
- The use of Commercial Of The Shelf (COTS) components in a radiation environment is a delicate point
- Extensive radiation tests required to characterize sensitivity to total dose, displacement damage, SEL, SEU
  - This is a significant amount of work
- It is difficult to get a guarantee that purchased components come from the same fab. with exactly the same technology as those circuits that have been radiation tested
  - Multiple fabs with slightly different details
  - Continuous fab and technology improvements
  - External 2nd. sourcing
- The fact that one chip from a family of chips have had no radiation problems is no guaranteed that the others will not
- Special radiation (space, military) qualified components are very expensive.

Optical links

Optical links

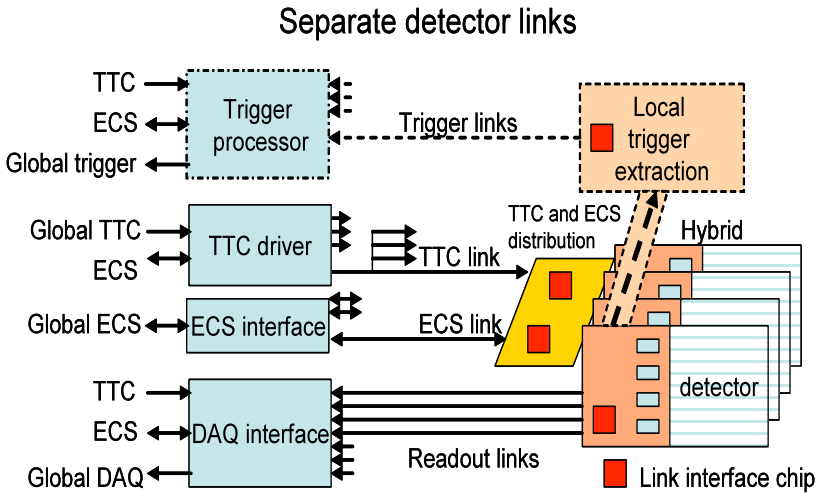
- High speeds
- Covers relatively easy distances needed for experiments: ~100m
- Galvanic isolation and no EMC/coupling problems
- High density cabling
- High density transmitters and receivers (e.g. 12 channels in snap12 module)
- Radiation effects on fibre, Laser and PIN
  - Appropriate components have been identified (e.g. VCSELS)
- Critical packaging (optical alignment) and fragile

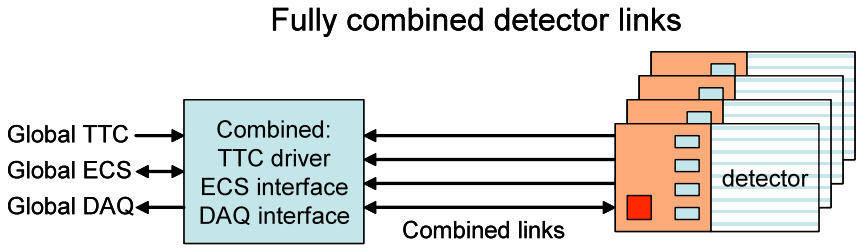




Separate or shared links

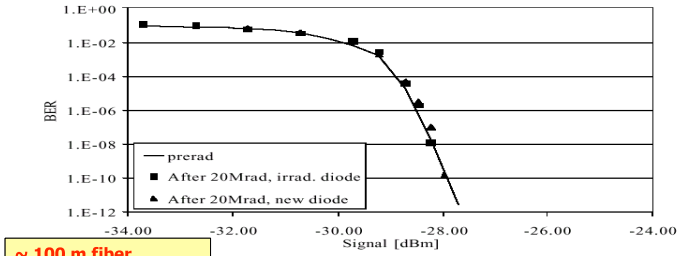
- There has been a tendency to keep the 3 (4) link types separate
  - Minimize interference
    - E.g. do not interrupt readout data flow when reading some monitoring information
    - Requirements for the three quite different
    - If the TTC or DAQ link does not work then one can at least diagnose problem via control and monitoring bus (but this part of the detector does still not work)
  - Three different cultures
    - Timing: hardware guys
    - Readout: DAQ guys
    - Control and monitoring: Slow control guys.
- Merged/shared
  - Modern optical links have so large bandwidth that a simple non interfering bandwidth sharing scheme can be used
  - Bus structures on its way out of computing (switched)
  - Each link only connects to small part of detector so failing link only implies loss of small detector part
  - Minimizes the number of interfaces to develop on front-end side and in counting house side

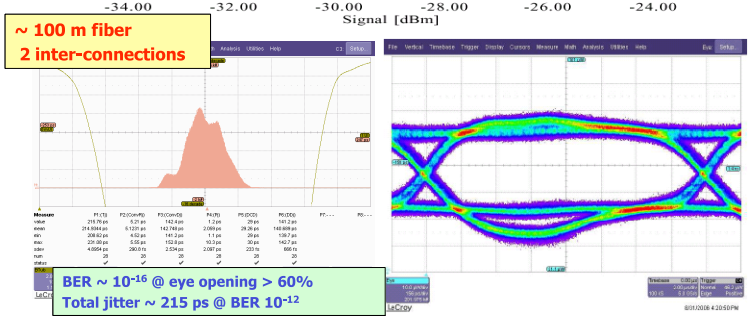


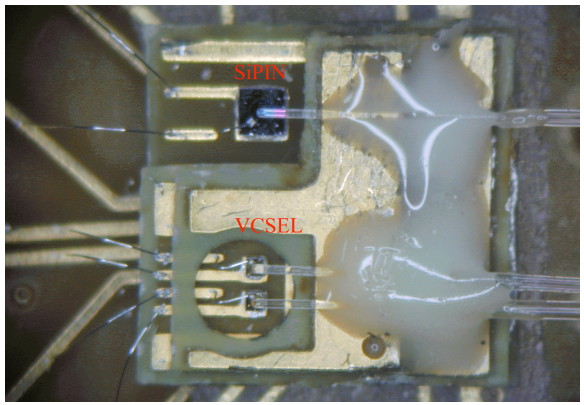


Digital optical links

- High speed: 1Ghz - 10GHz – 40GHz
- Extensively used in telecommunications (expensive) and in computing (“cheap”)
- Encoding
  - Inclusion of clock for receiver PLL’s
  - DC balanced
  - Special synchronization characters
  - Error detection and or correction
- Reliability and error rates strongly depending on received optical power and timing jitter
- Multiple (16) serializers and deserializers directly available in modern high end FPGA’s.

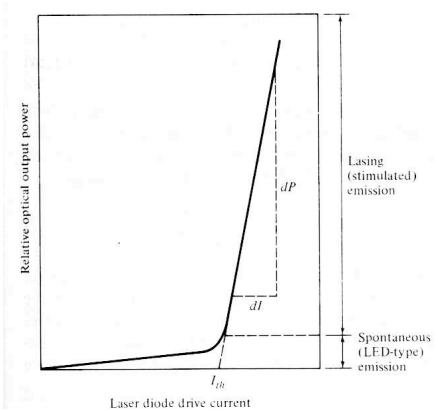


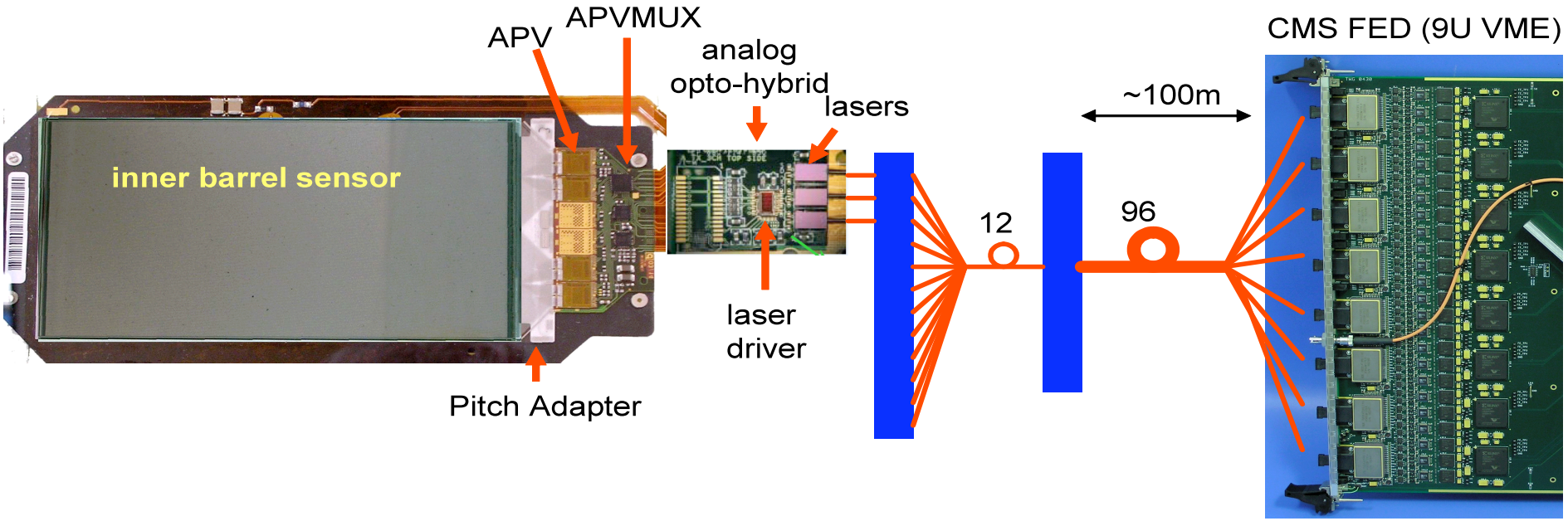




Analog optical links

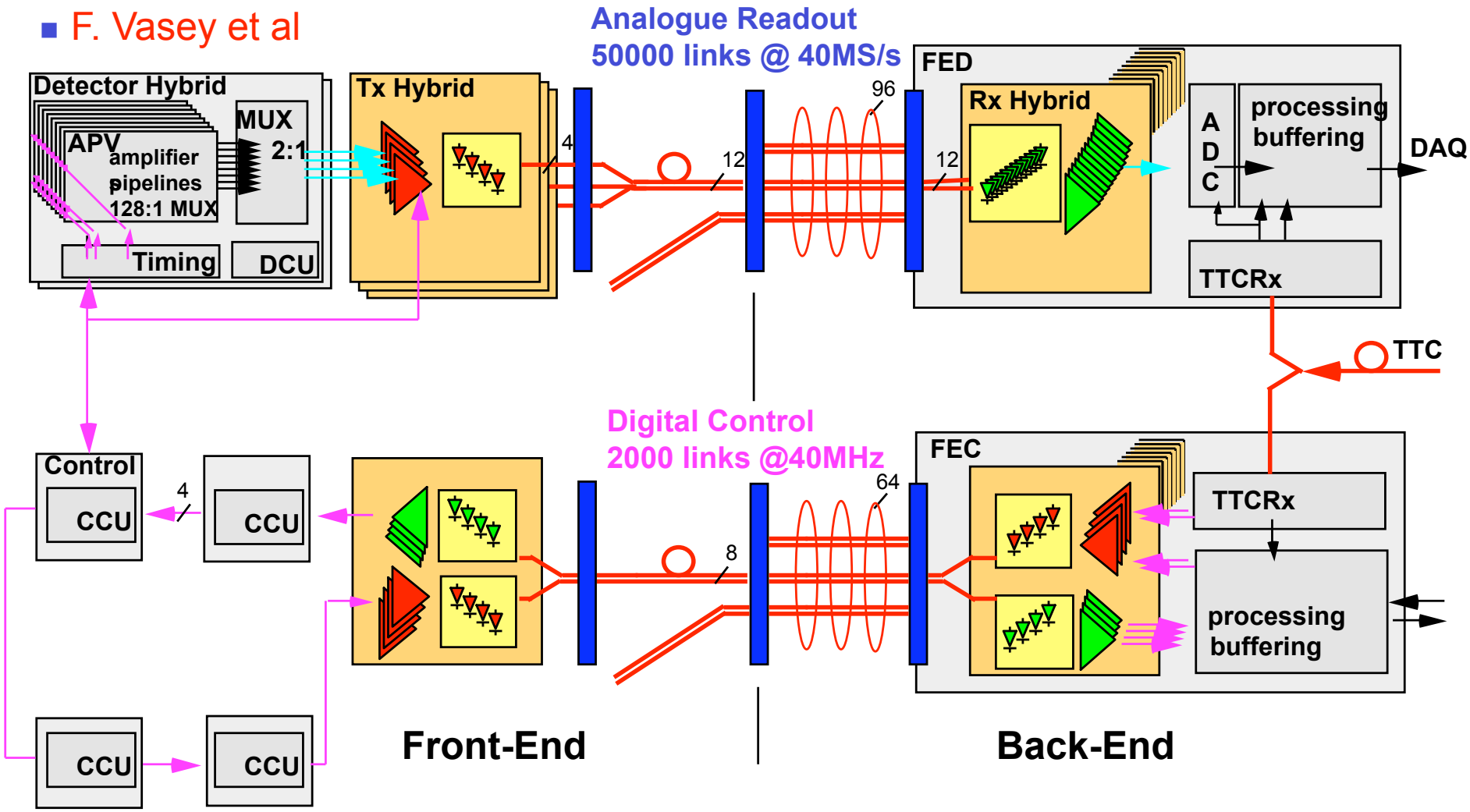
- Used in large quantity for CMS silicon tracker with analog readout
  - 50 k links
  - ~8 bits dynamic range x 40 Msamples/s = 320 Mbits/s
- Not mainstream technology so the design and use of such a link is non trivial (in house development)
  - Prevents the need for radiation hard ADC's in the front-end electronics (Low power ADC's with small area and low power are today available)





CMS Tracker readout and control

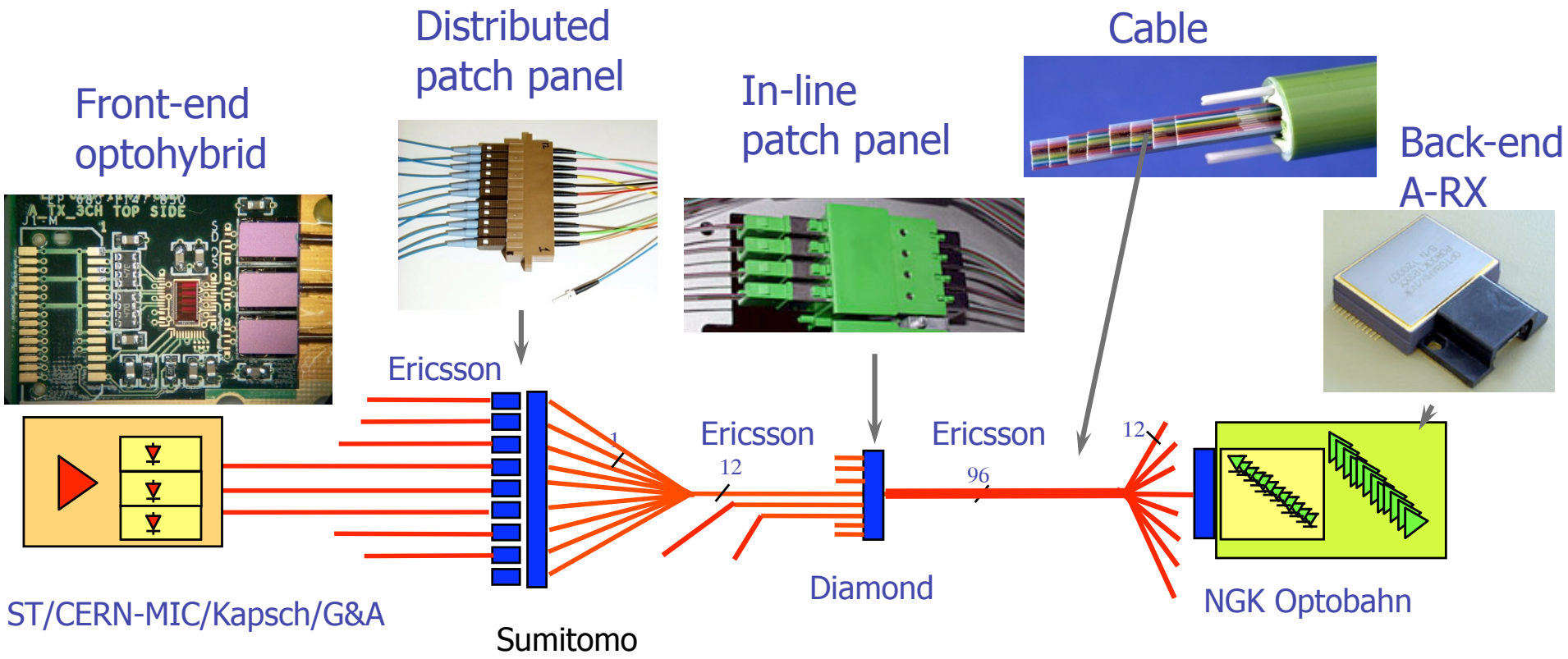
- F. Vasey et al



http://cms-tk-opto.web.cern.ch/cms-tk-opto/

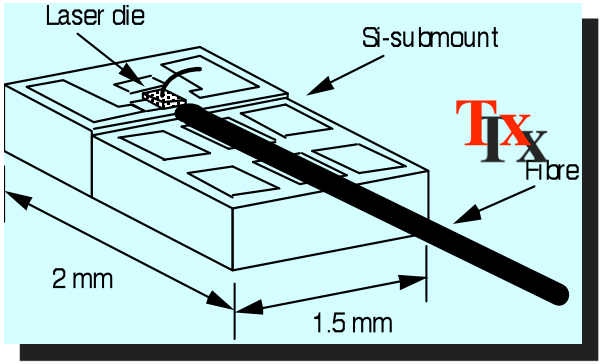
CMS Tracker analogue optolinks

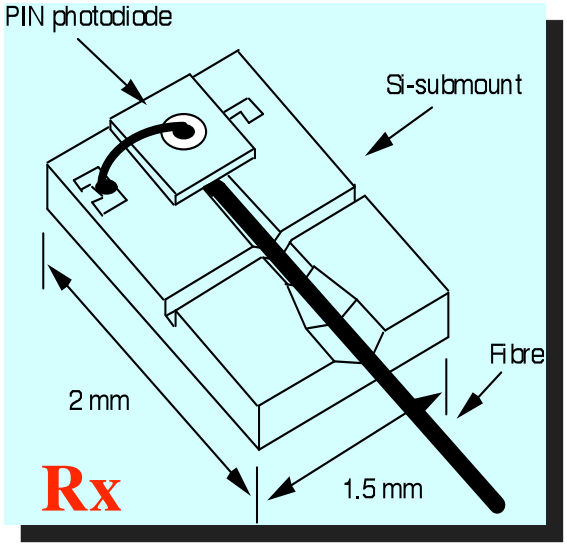
- COTS-based parts produced to CMS specifications
  - Production and assembly all done commercially
  - Qualification and final (sampled) acceptance done by CMS
  - Tracker requires miniature connectors, and care with handling



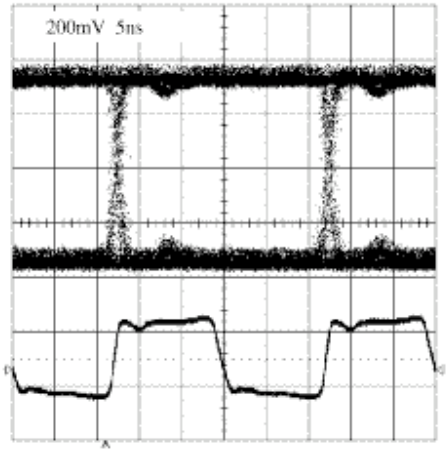
CMS Tracker Tx and Rx

- Edge emitting 1.3μm InGaAsP MQW laser diodes
  - single mode fibre ~50mW/256 detector channels
  - Tx: laser actively aligned, in hermetic package
  - Rx: fibre aligned by V-groove, with etched mirror



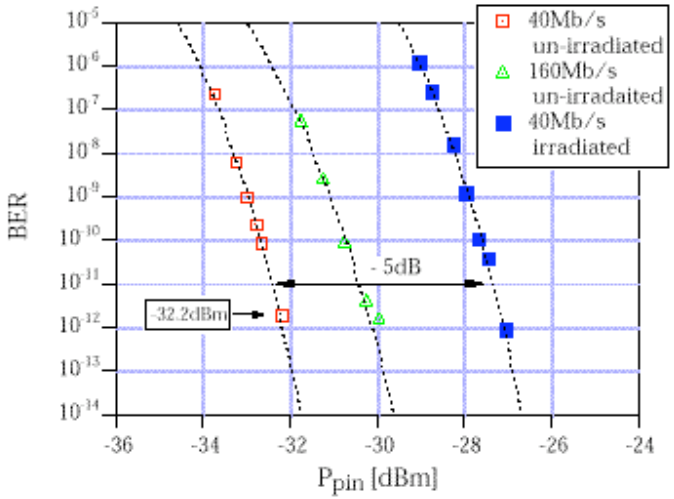


Eye Diagram (@40Mb/s)



BER = 10^{-12} @ P_{pin} = -32.2dBm (0.6 μW)

Bit Error Rate



same components for digital control BER << 10^{-12}

Off-detector electronics

Readout

- Large amount of data to bring out of detector
  - Large quantity: ~100k in large experiment
  - High speed: Gbits/s
- Point to point unidirectional
- Transmitter side has specific constraints
  - Radiation
  - Magnetic fields
  - Power/cooling
  - Minimum size and mass
  - Must collect data from one or several front-end chips
- Receiver side can be commercially available module/components (use of standard link protocols when ever possible)

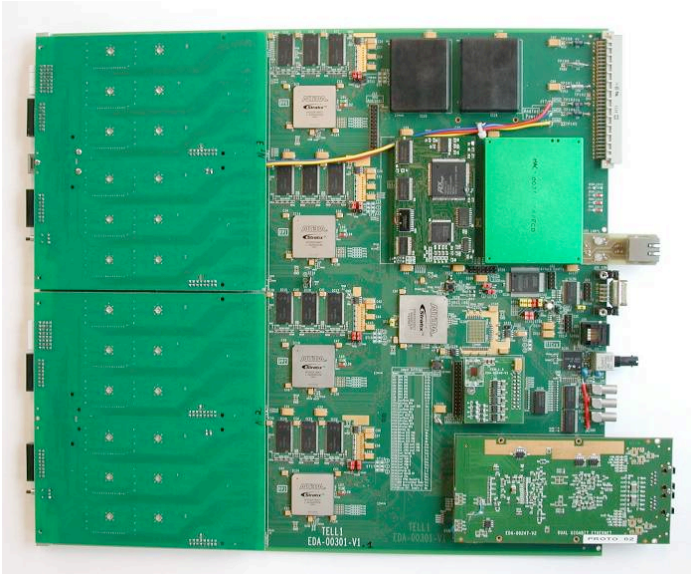
DAQ interfaces

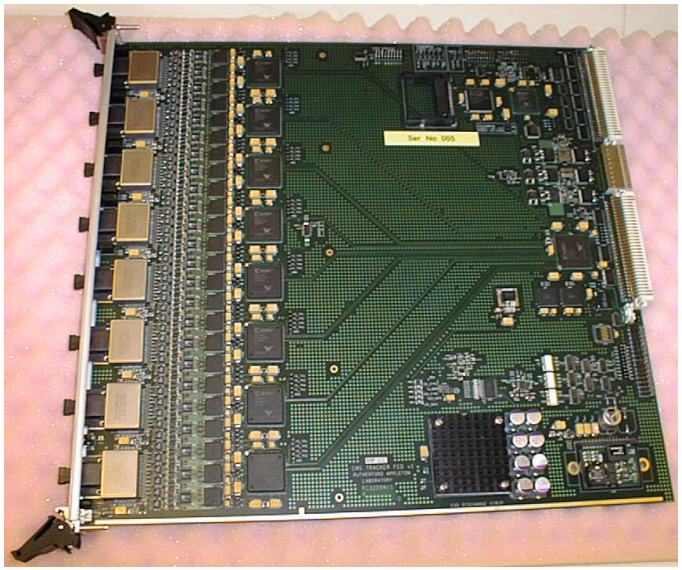
- Front-end data reception
  - Receive optical links from multiple front-ends: 24 - 96
  - Located outside radiation
- Event checking
  - Verify that data received is correct
  - Verify correct synchronization of front-ends
- Extended digital signal processing to extract information of interest and minimize data volume
- Event merging/building
  - Build consistent data structures from the individual data sources so it can be efficiently sent to DAQ CPU farm and processed efficiently without wasting time reformatting data on CPU.
  - Requires significant data buffering
- High level of programmability needed
- Send data to CPU farm at a rate that can be correctly handled by farm
  - 1 Gbits/s Ethernet (next is 10Gbits/s)
  - In house link with PCI interface: S-link

Requires a lot of fast digital processing and data buffering: **FPGA's**, DSP's, embedded CPU

Use of ASIC's not justified

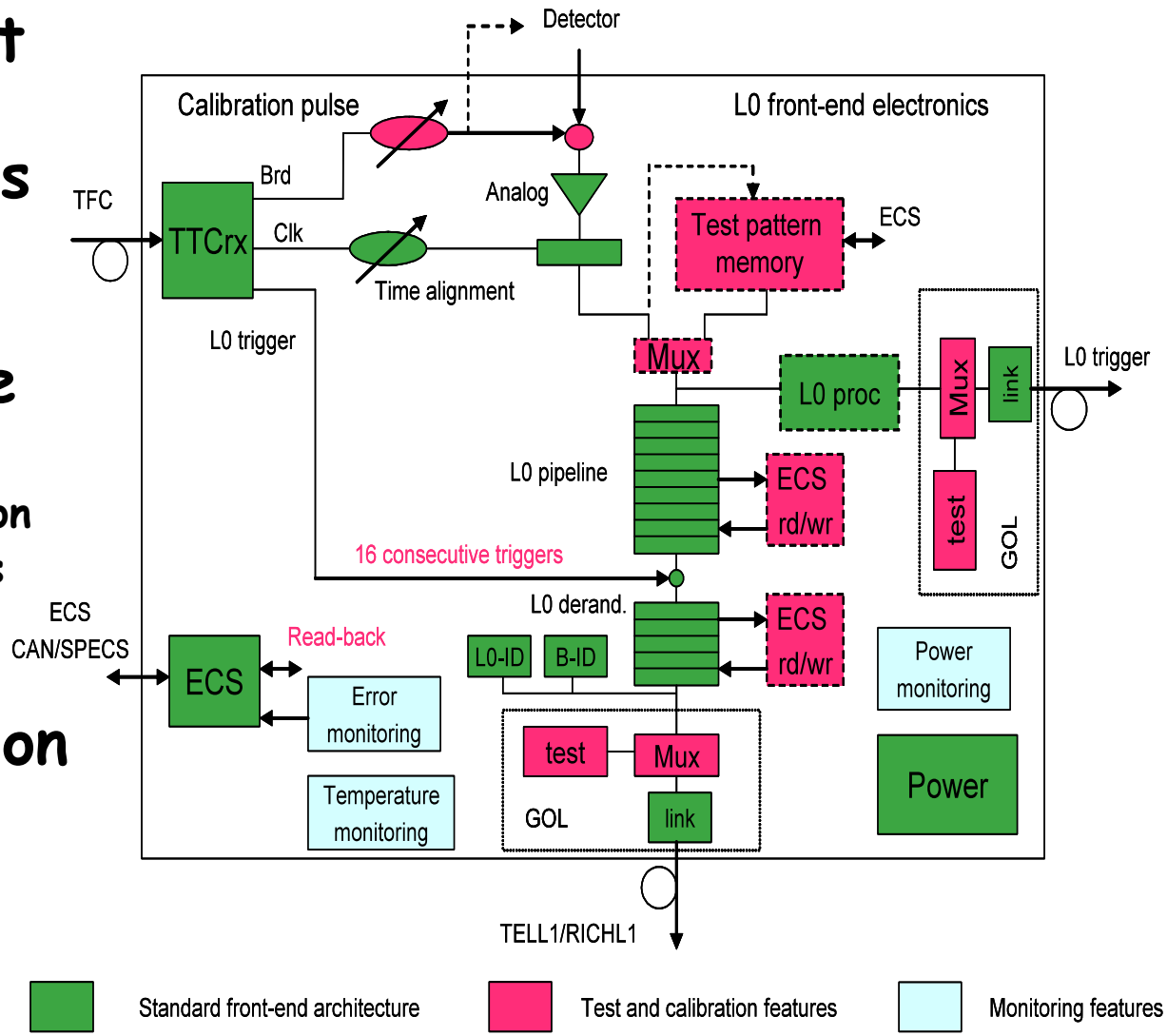
Complicated modules that are only half made when the hardware is there: FPGA firmware (from HDL), DSP code, on-board CPU software, etc.





Calibration and test

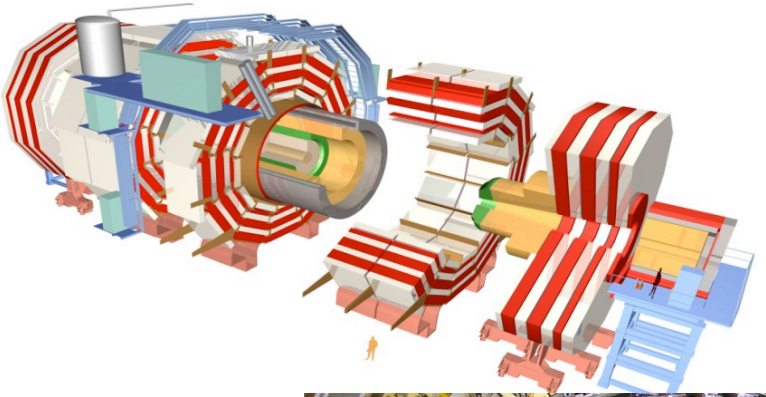
- Front-end systems needs extended set of testing and calibration features to allow in-situ verification of modules and all the interconnections
  - Calibration pulse injection
  - Test pattern generators
  - Read/write access to embedded buffers
- Amplitude calibration
- Time alignment
- Local monitoring
- Etc.

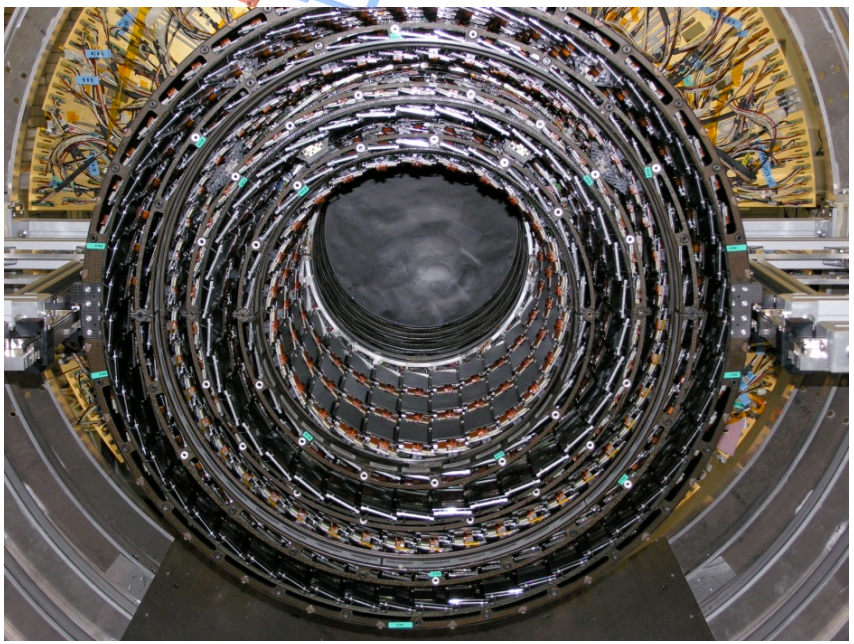


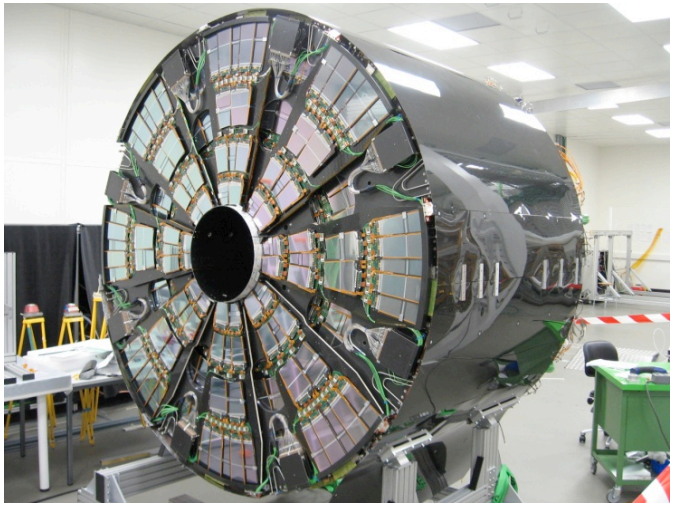
Specific examples

CMS tracker

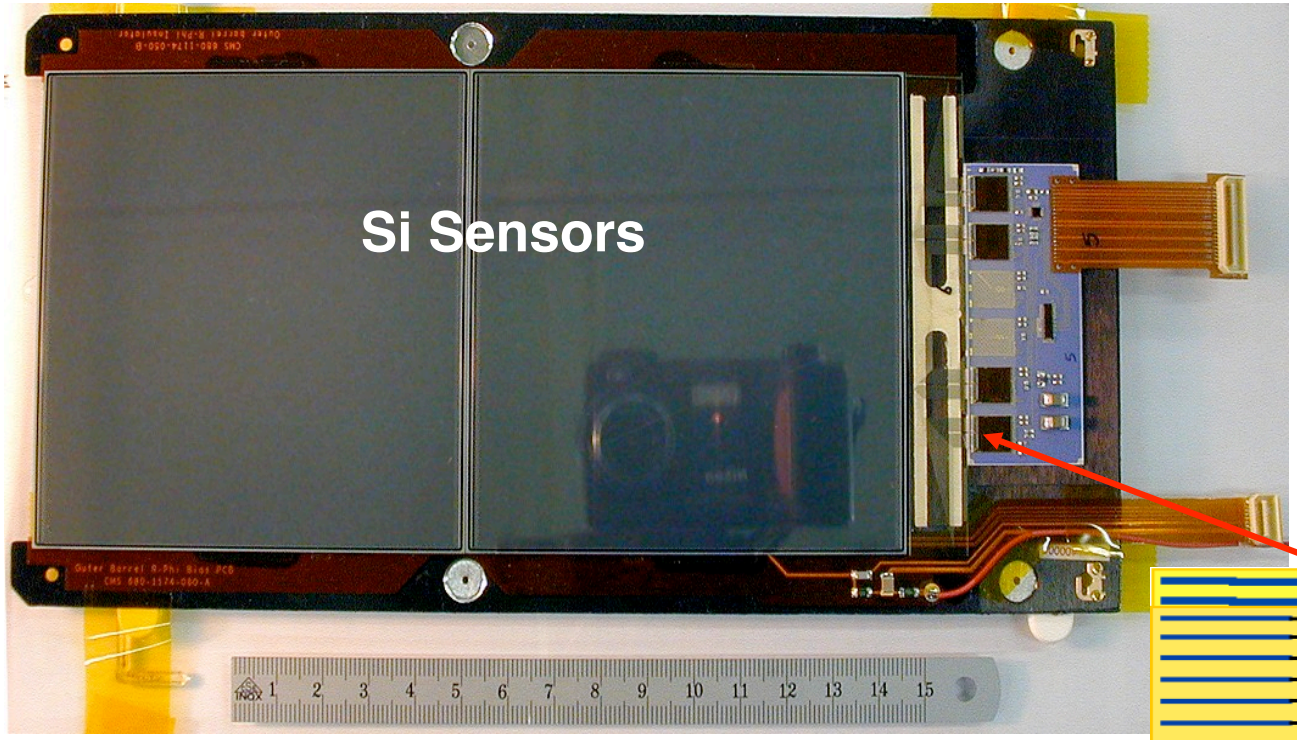
- 10M channels
- Relatively slow analog shaping: 50ns
- Analog pipeline
- Switched capacitor deconvolution after trigger acceptance
- Analog optical links
- Digitization at link receiver





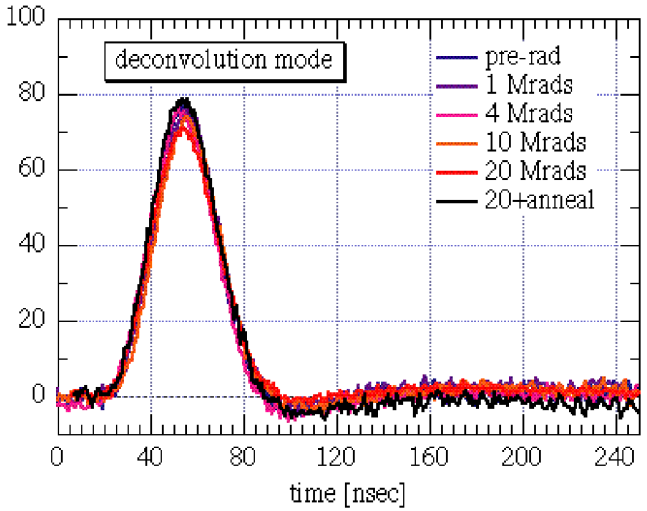


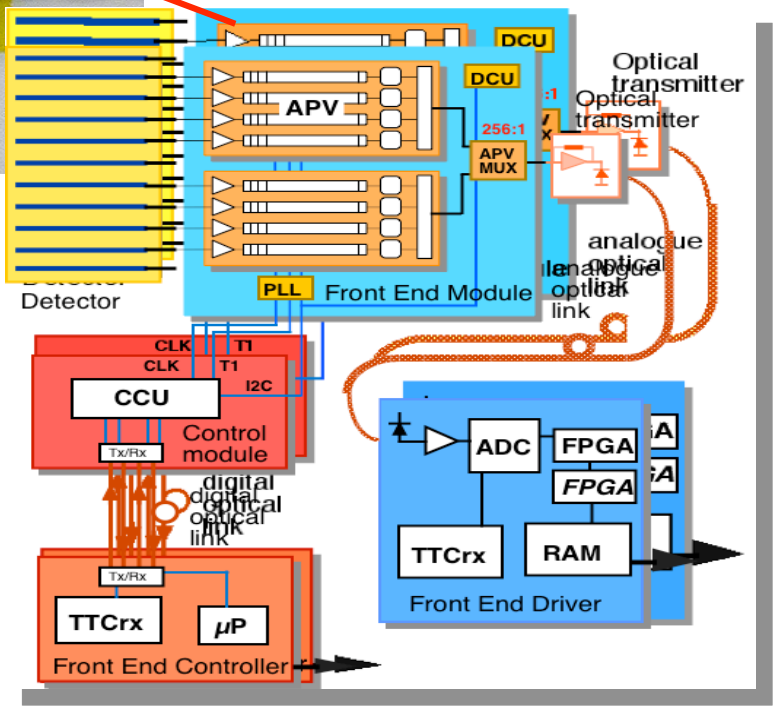
Si Modules and Electronics Chain



Main features:
Analogue readout
No on-detector zero suppression
Optical analogue data transfer
Control signals sent optically
Local electrical transfer

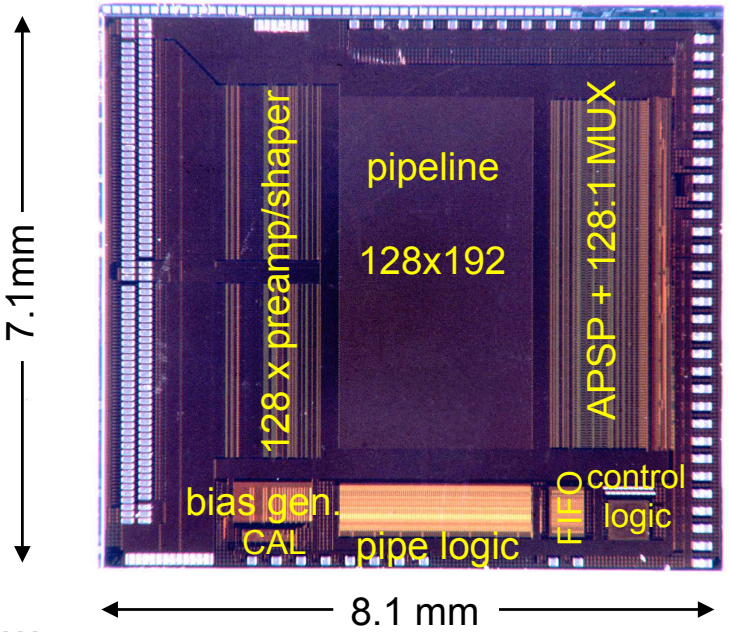
Only 0.25µm ASICs
APV25
~100,000 die, inc spares
Complete control system
5000 - 20000 die of:
DCU, PLL, CCU, LD…
LVDSbuf/mux

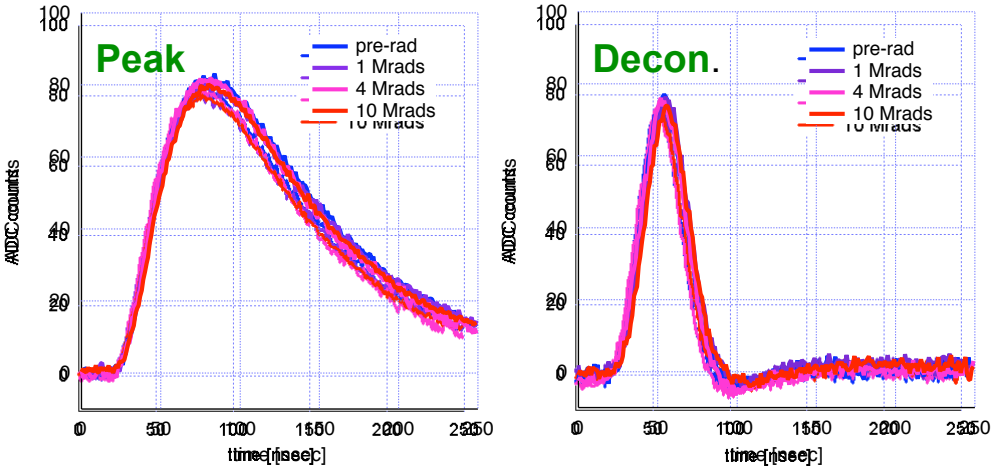


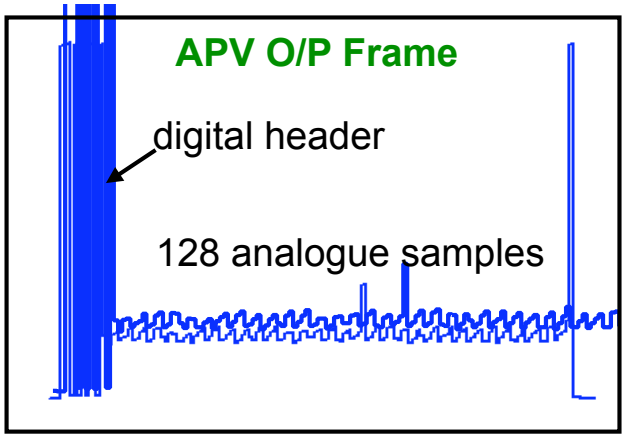


APV25

- Main features
  - 128 readout channels
  - 50 ns CR-RC amplifier
  - 192 cell pipeline memory
  - alternate operating modes
    - peak, deconvolution, multi-mode
    - on-chip analogue signal processing
  - on-chip ancillary functions
    - eg calibration, I^2C, programmable latency…

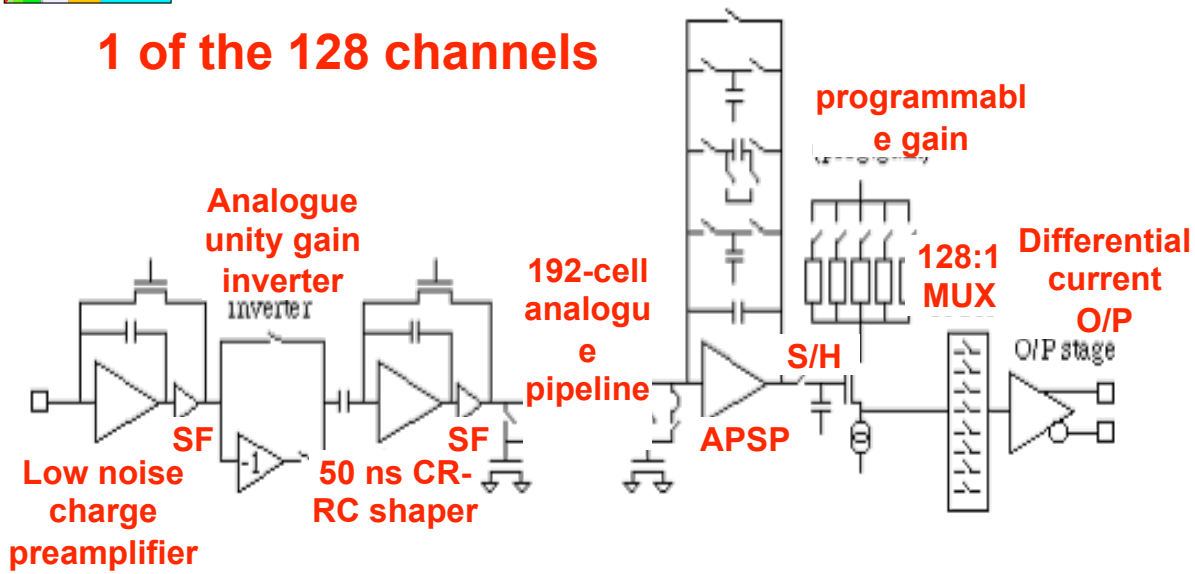


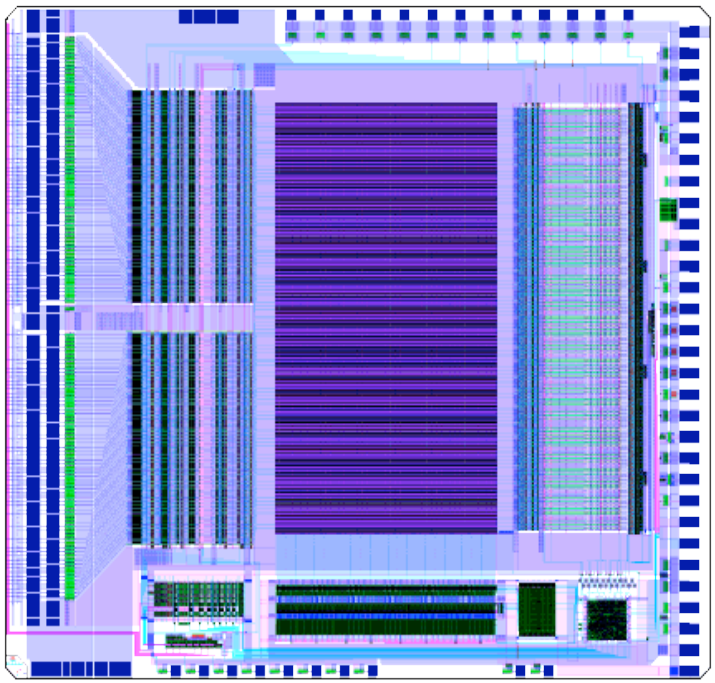


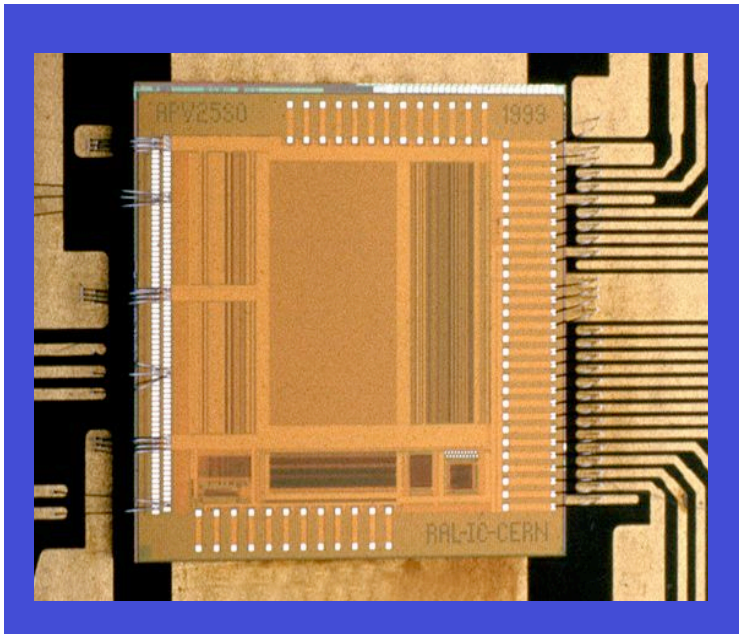


APV25 0.25μm CMOS

1 of the 128 channels







APV25-S0 (Oct 1999)

Chip Size 7.2 x 6.5 mm

APV25-S1 (Aug 2000)

Chip Size 7.1 x 8.1 mm

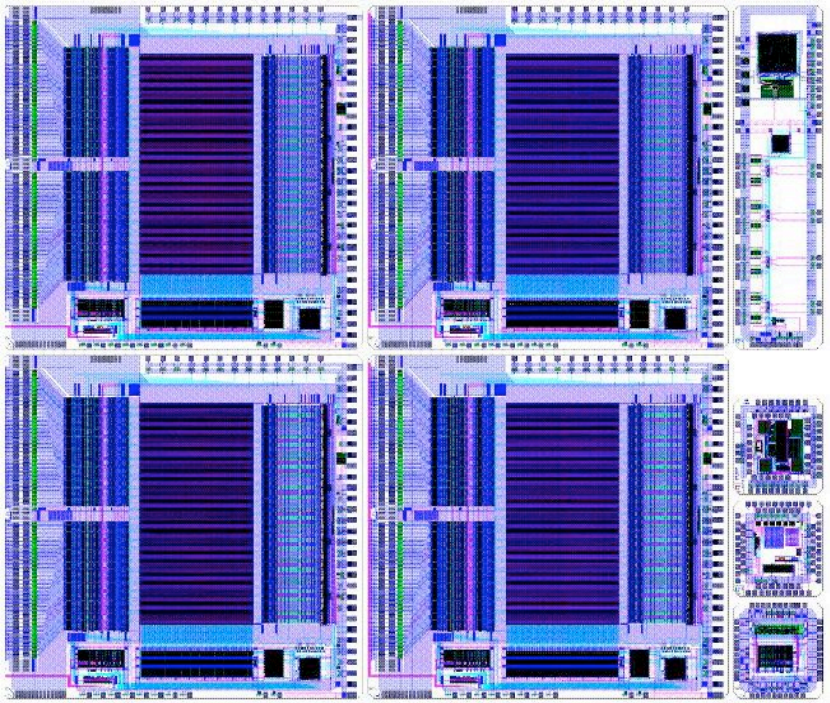
Final

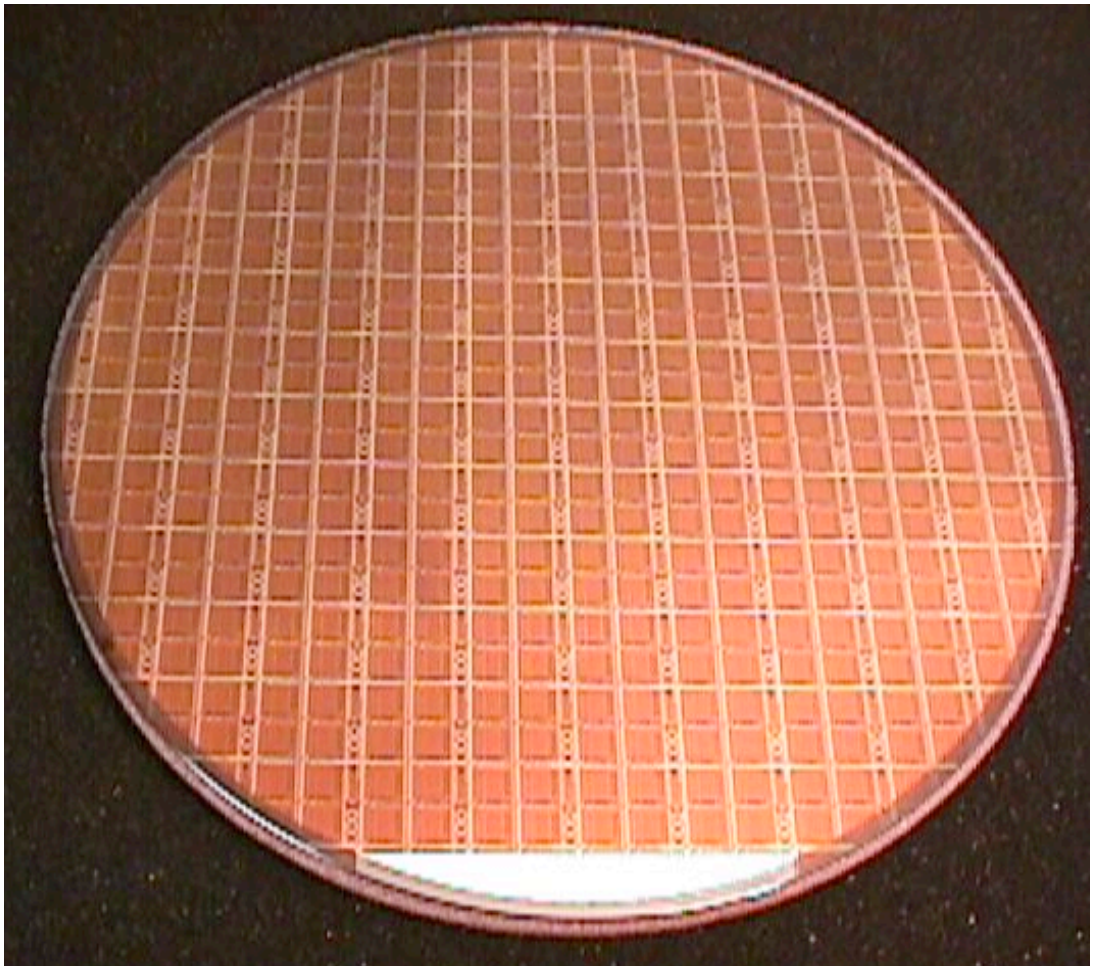
Production wafer layout

- Overall size 200mm
- APV25 die ≈ 380
- APVMUX+PLL die ≈ 100

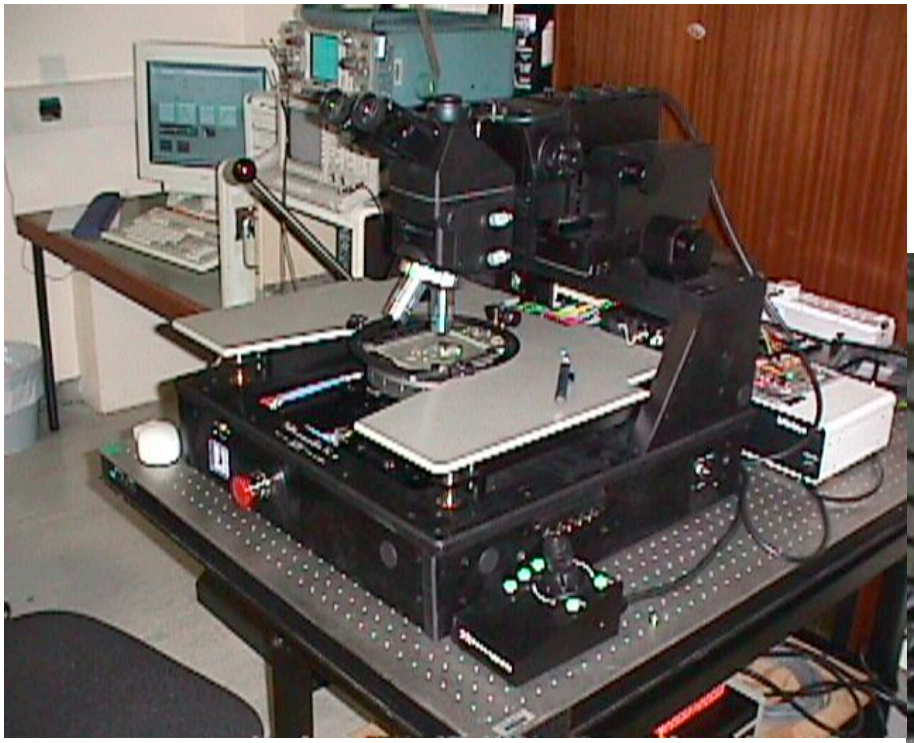
Reticle dimensions

18,420mm x 14,400mm





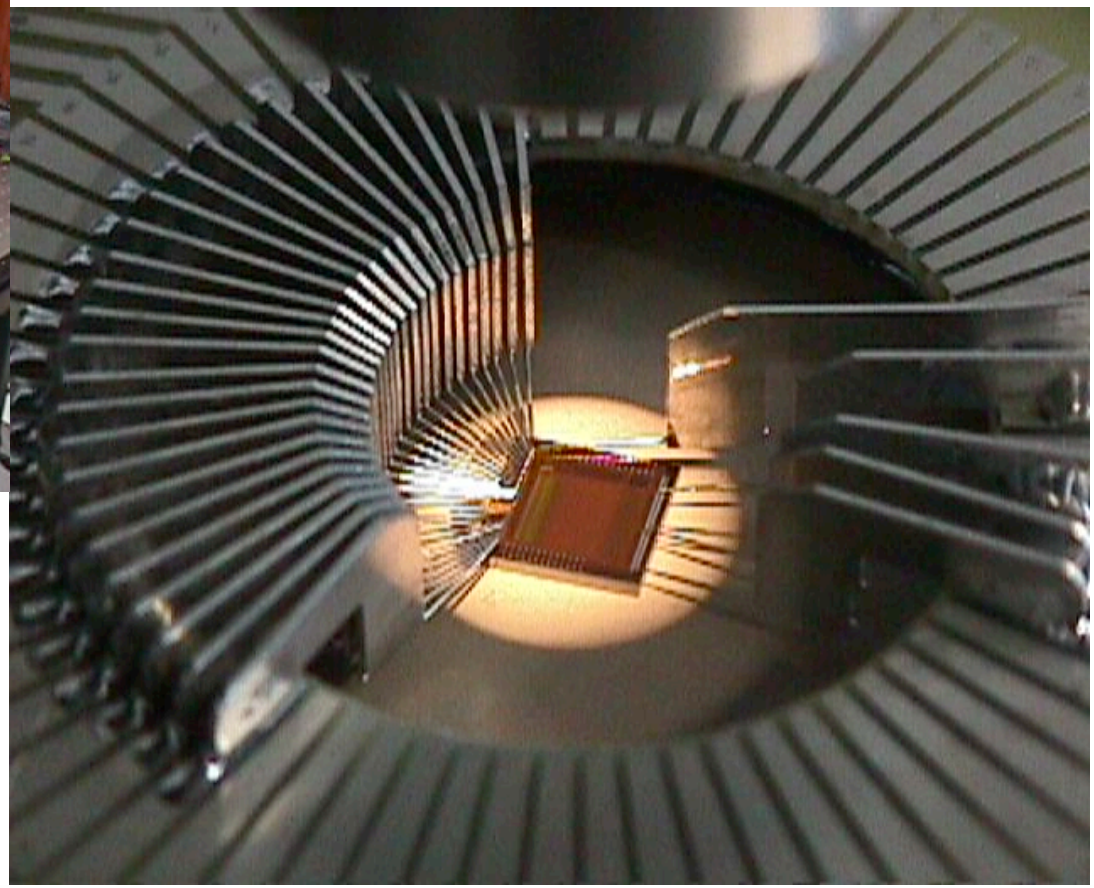
Chip testing



- Automated on-wafer testing

  proven on 4inch APV6 wafers

  presently using APV25 die



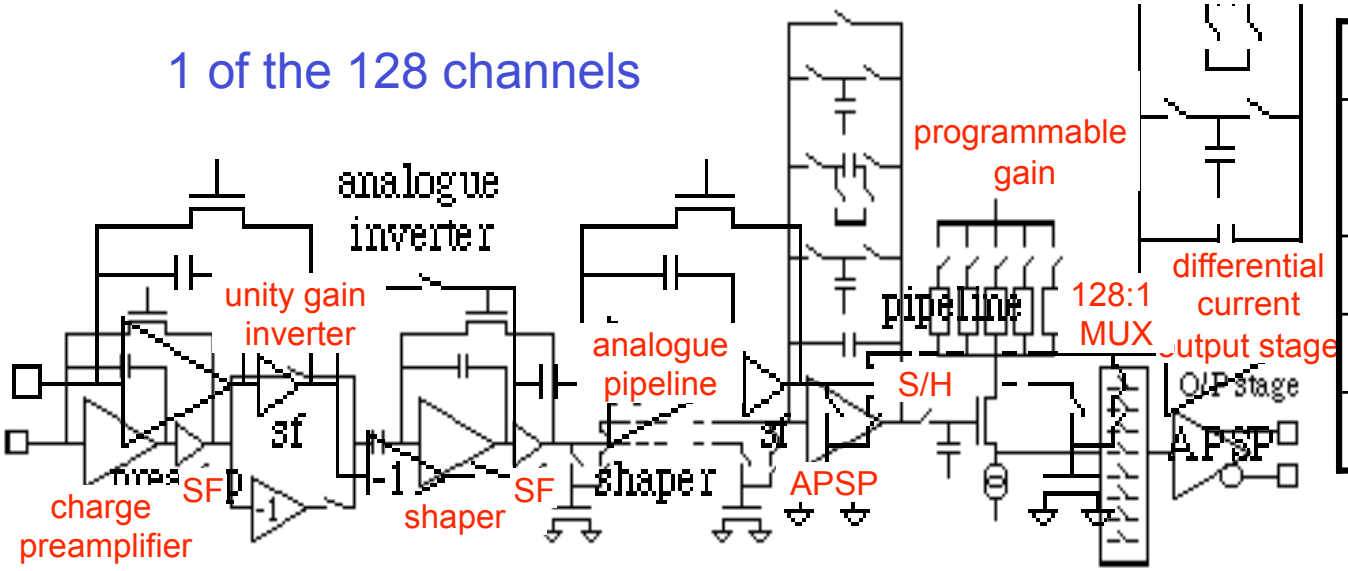
- Operational at Imperial College

  Second set-up at RAL

APV25 design

V_{supply}	0 - 2.5V
Power/channel	1.9mW analogue + 0.4mW digital
Input transistor	pMOS W/L= 2000/0.36 I_{DS} = 400µA
Filtering	50ns CR-RC or 3 weight analogue sum (deconvolution)
Pipeline length	192 cells, including 32 [max] cells readout buffer

1 of the 128 channels

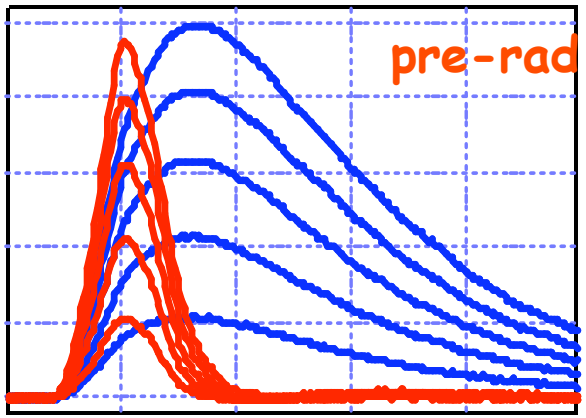


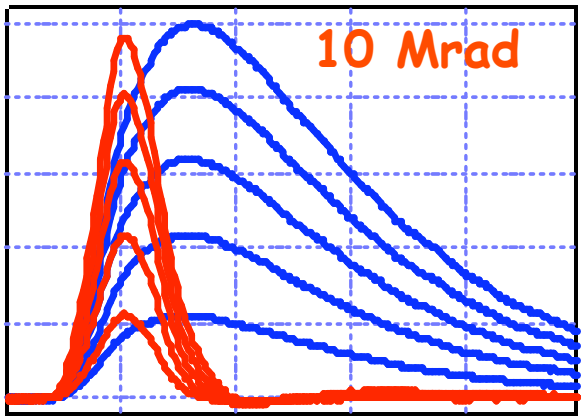
Analogue power	mW
Preamplifier + buffer + inverter	0.90
Shaper + buffer	0.25
APSP	0.20
OP & MUX	0.54

M. Raymond
Imperial College

APV25 irradiation results

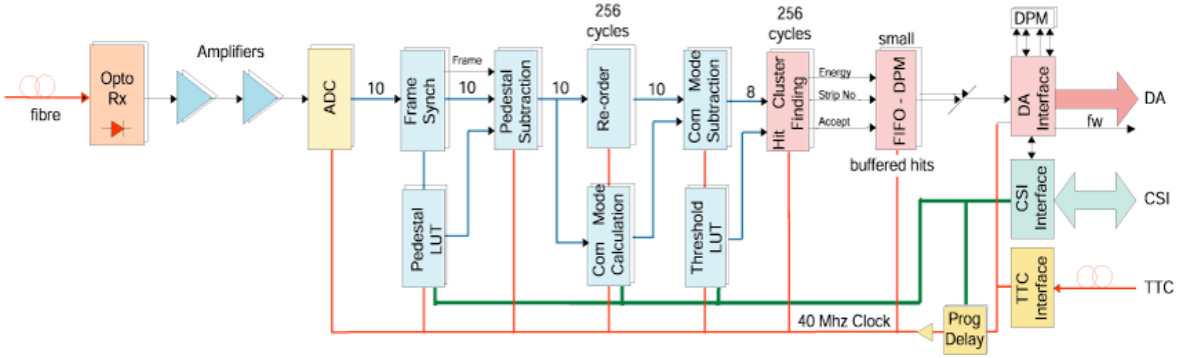
- Only minor effects after irradiation
  - Compensated for by minor tuning of parameters at long intervals during operation





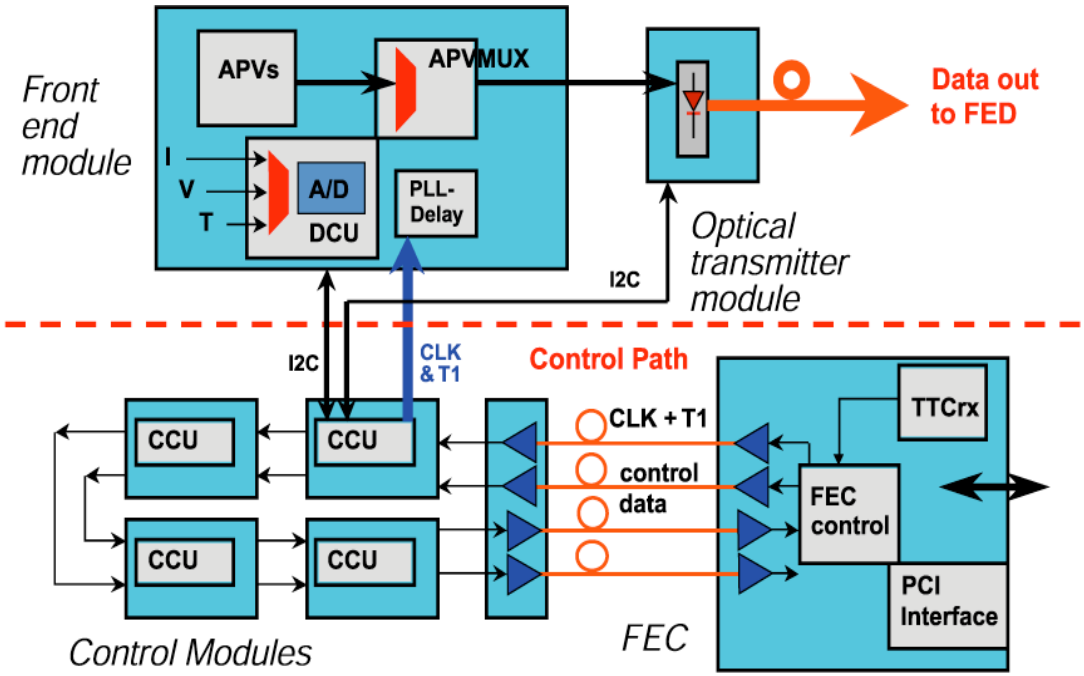
Front-end Driver

Pulse height data are received by a photodiode-amplifier on the Front End Driver which digitises and processes the signals, including reordering and pedestal subtraction, and stores results in a local memory for the higher level data acquisition. In high luminosity conditions when CMS is operating at the maximum trigger rate, cluster finding will be carried out on the FED to reduce the data volume



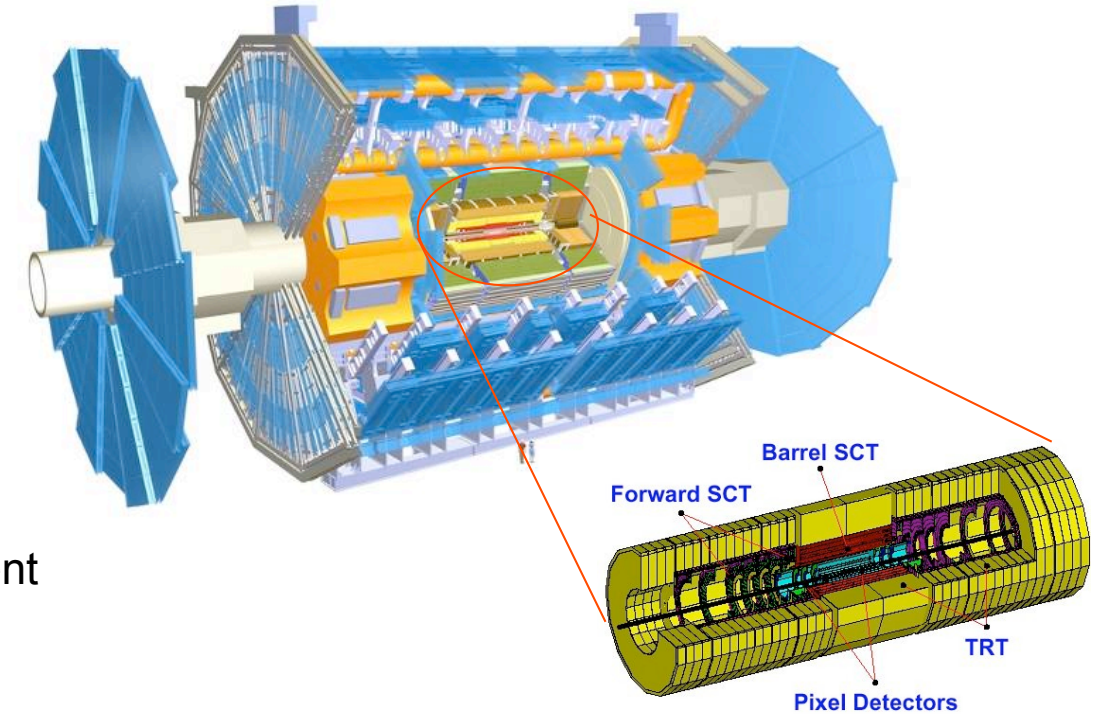
Control System

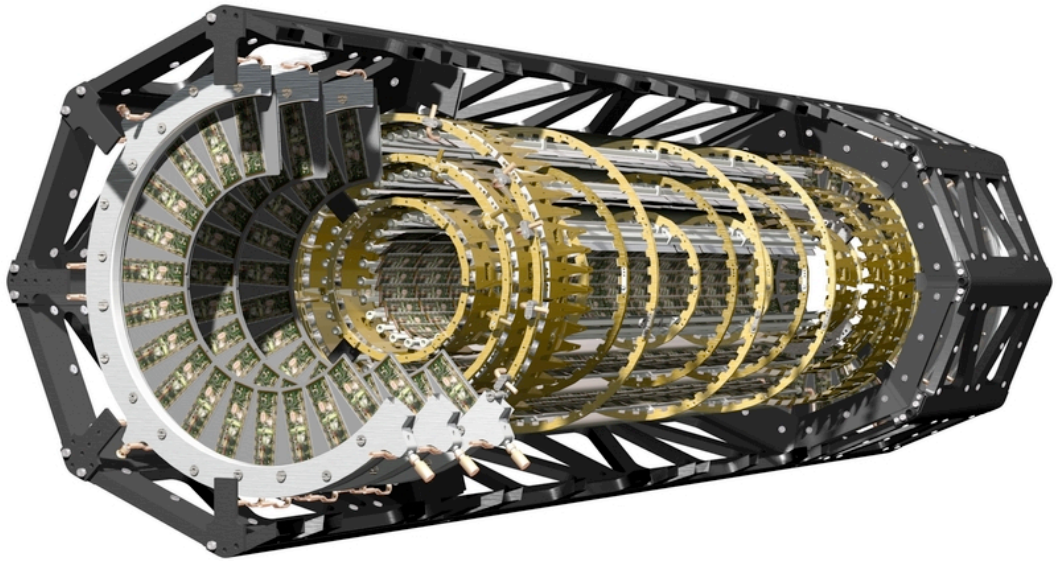
The Front End Controller supervises control and monitoring of the front-end electronics and is the interface to the CMS Timing Trigger and Command system. Digital optical links, using the analogue link components, transmit triggers, clocks and control data. Internally, digital transitions are recovered by photodiode-amplifiers and distributed electrically by a Communication and Control Unit (CCU) to detector modules. Clocks are recovered by Phase Locked Loop (PLL) chips on each module for high reliability and minimum phase jitter. CCU modules can be configured as rings to match the tracker topology and reduce cost

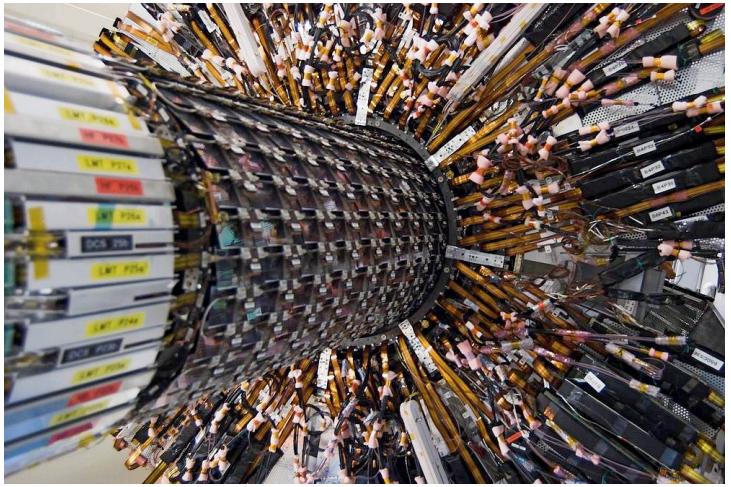


ATLAS tracker

- Strips: 6M
  - Binary system
  - 128 channels per chip
  - pipeline
  - Threshold adjust per channels
- Pixels:80M
  - Storage of time stamps
  - TOT amplitude measurement



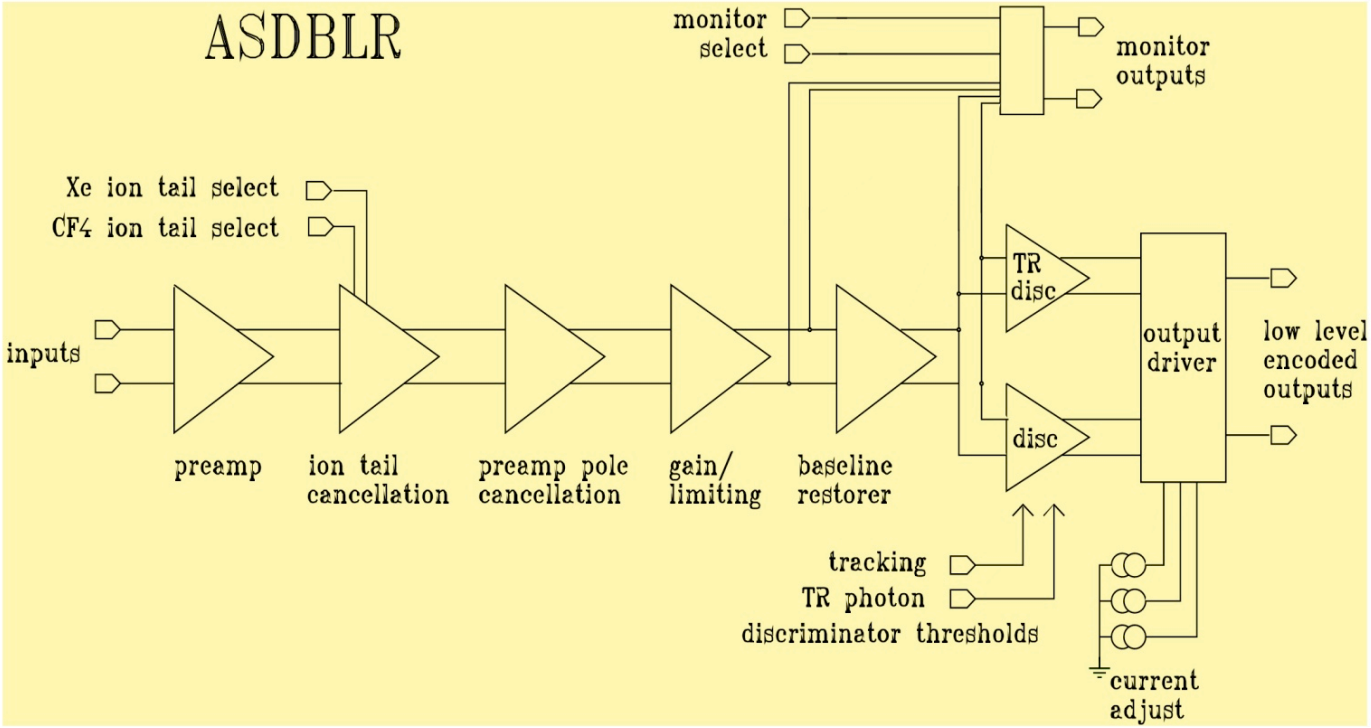




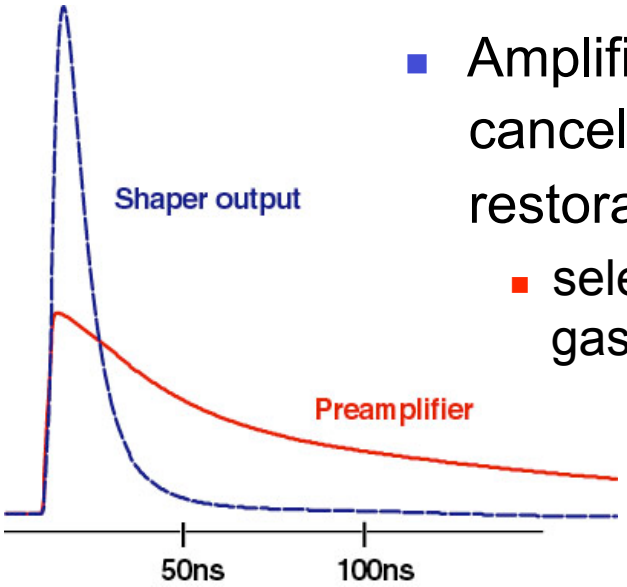
ATLAS TRT readout

- ASDBLR 8 channel amplifier/shaper/discriminator/BLR
  - DMILL 0.8μm hardened BiCMOS
  - peaking time 7-8ns to reduce pileup
  - requires speed and stability, since high occupancy
  - and baseline restorer to maintain stable threshold levels
  - two level discriminator => electron identification

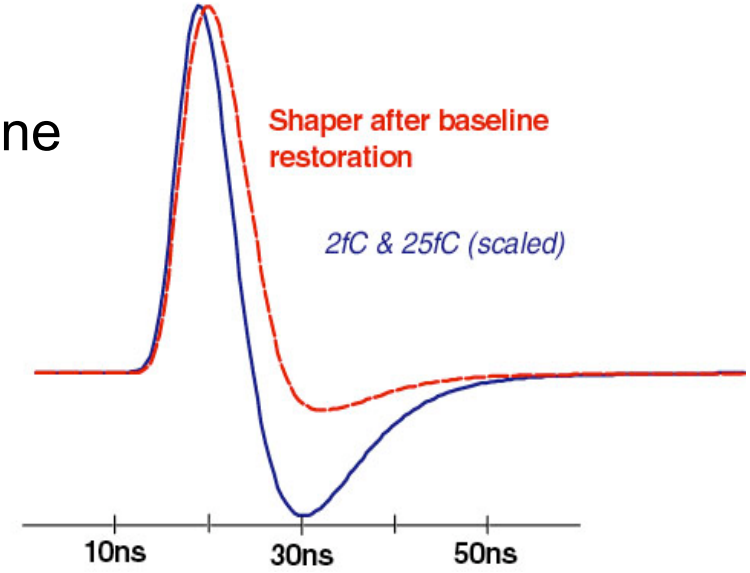
- + DTMROC-S pipeline and timing measurement *16chan/chip*
  - 0.25μm CMOS

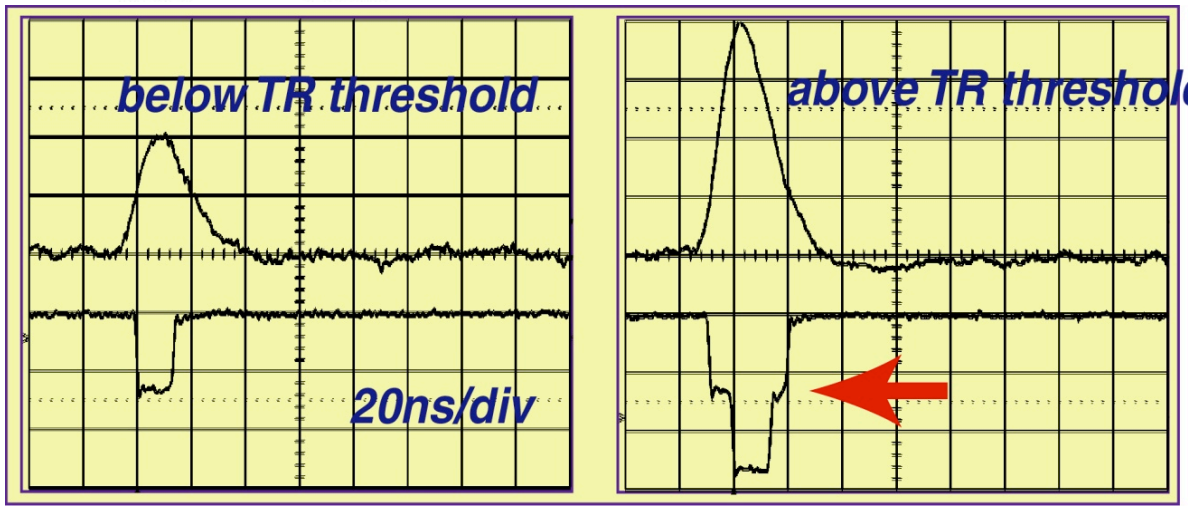


ATLAS TRT ASDBLR front end



- Amplifier provides tail cancellation and fast baseline restoration
  - selectable for CF_4 and Xe gas mixtures

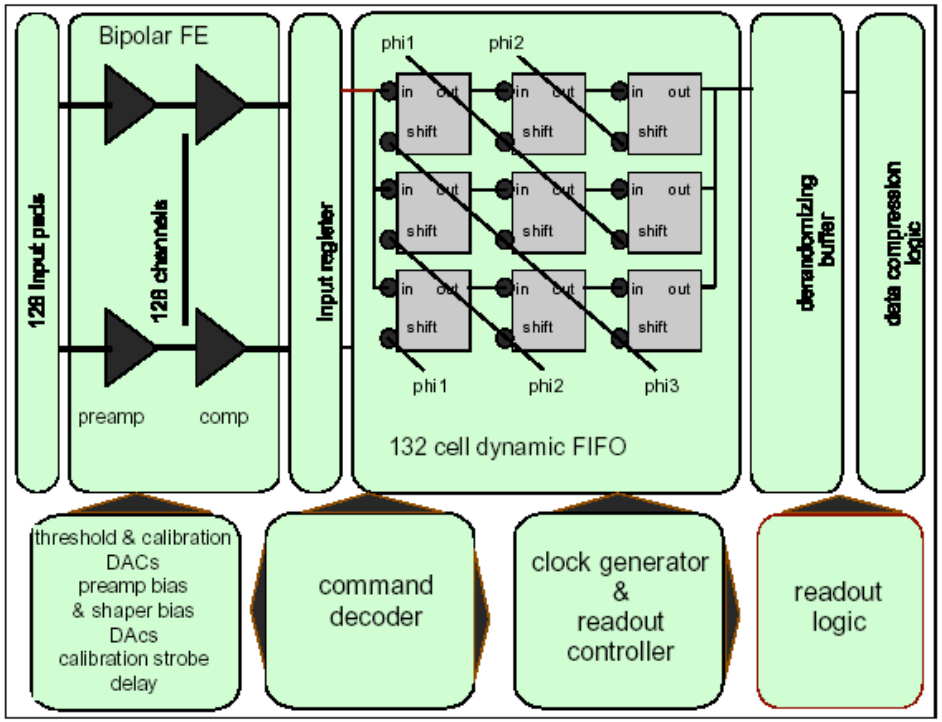




4mm straw + Xenon based gas

ATLAS SCT front end

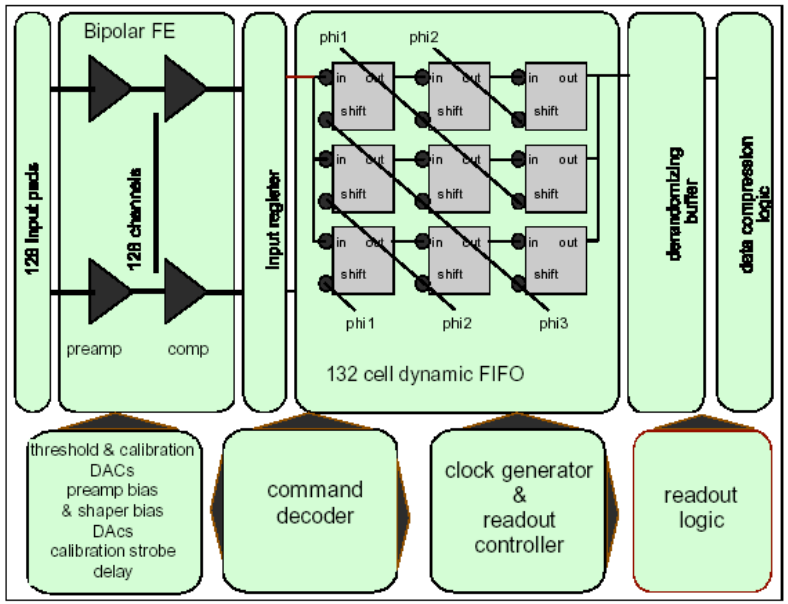
- Binary readout
  - 128 channel in DMILL BiCMOS
  - AC coupled input
  - 6M thresholds, so require good uniformity in discriminator threshold
    - achieved with Trim DAC
  - care to avoid common mode noise

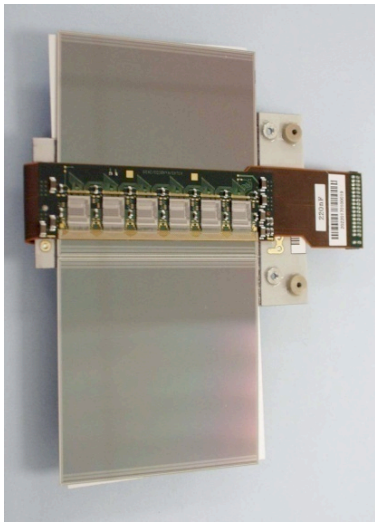


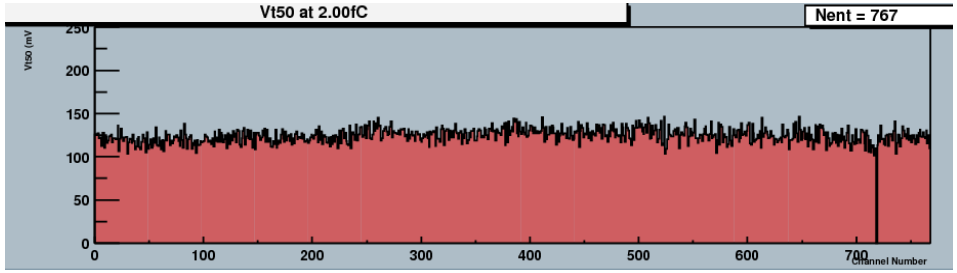
ABCD3T

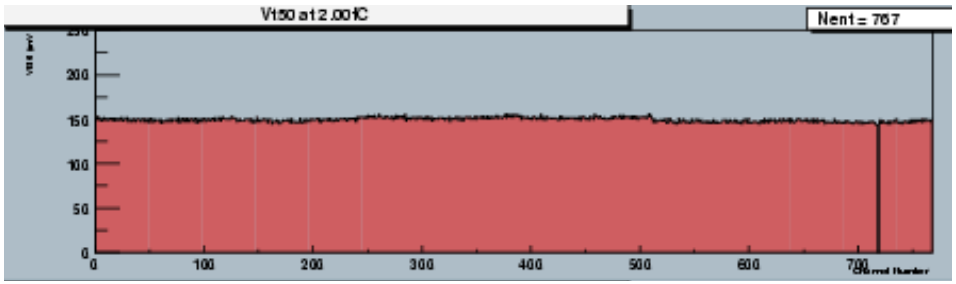
- Some specifications…
  - Peaking time 20ns
  - Timewalk <16ns
  - ENC < 1500e for non-irradiated module
  - Linearity better than 5% for 0 - 4fC
  - Threshold correction 4 ranges (DAC) with 10% absolute accuracy
  - Double pulse resolution 50ns after 3.5fC signal

ATLAS silicon strip







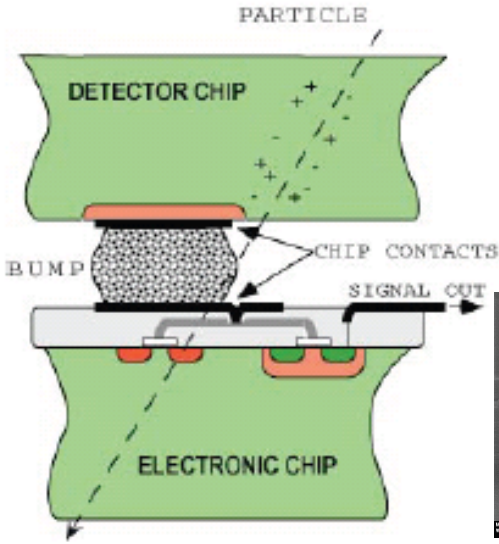


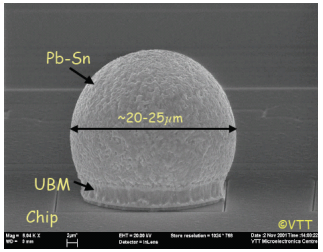
Before individual threshold adjust

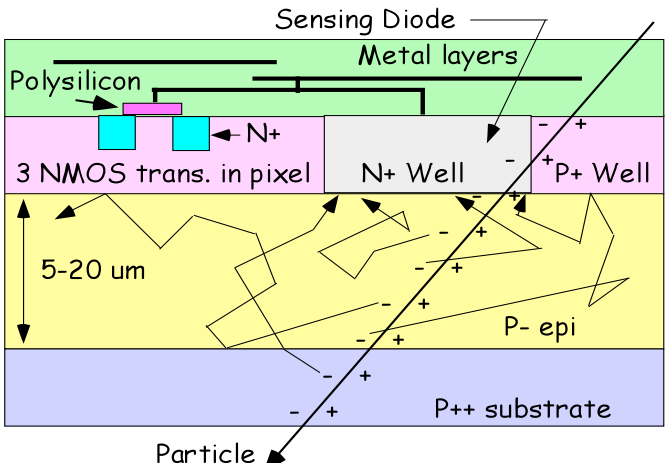
individual adjusted

Pixels

- Separate detector with bump bonding
  - Bump bonding pitch and yield critical
  - Not compatible with standard bump bonding used to connect chips to IC packages.
- Same silicon substrate as electronics (dream/nightmare ?)
  - Use of silicon substrate below electronics as detector: Monolithic Active Pixel Sensor (MAPS)
  - No dead spots allowed in HEP (not like a CMOS camera sensor that can allocate part for electronics and other part for photon detector within pixel !.
  - Silicon substrate used for electronics chips in most cases far from ideal as silicon detector
  - Connection to the detector in the substrate and get sufficient charge collection (and speed) efficiency

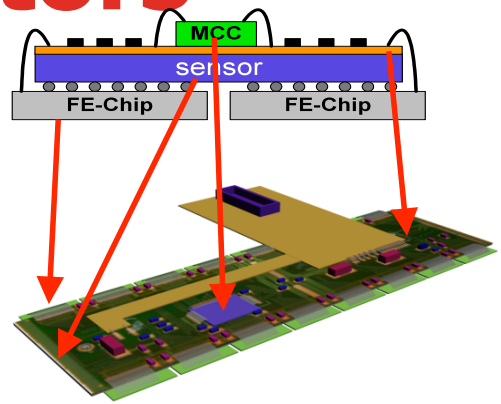


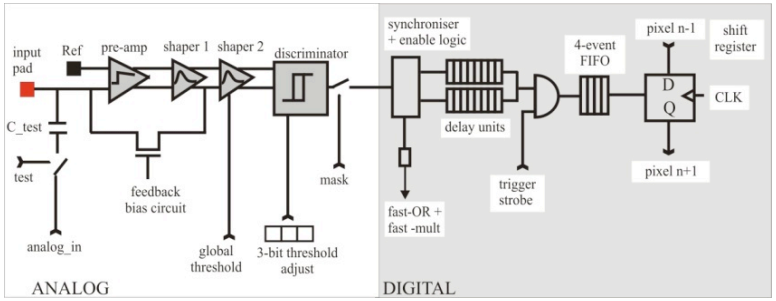


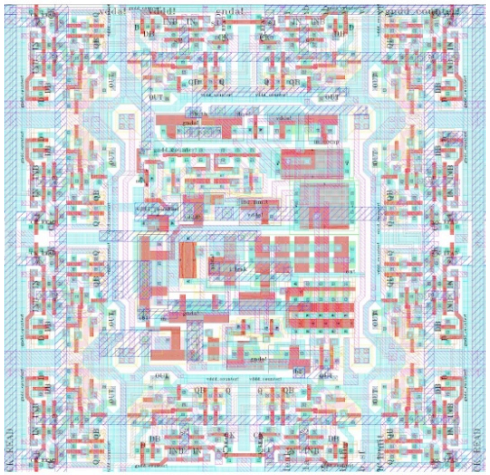


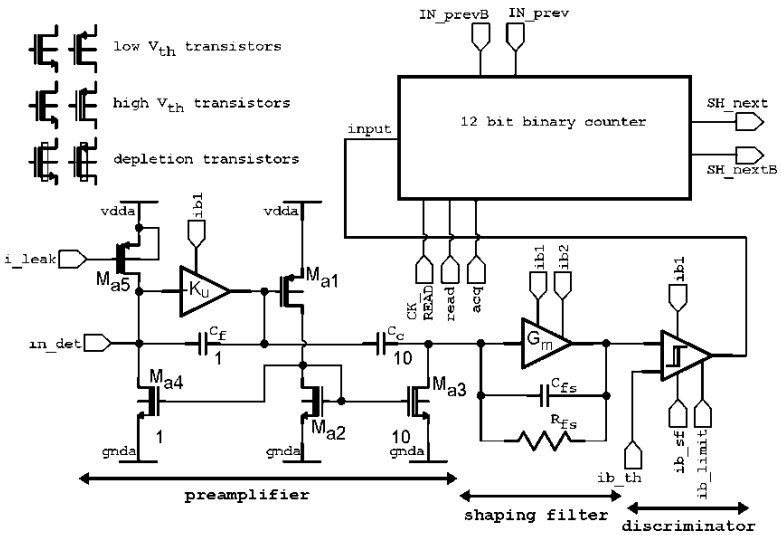
Pixel detectors

- Very tight coupling between electronics and detector.
  - Detector - electronics connection critical (bump bonding)
- Very limited area available for channel electronics
  - Pre-amp, shaper, discriminator, (buffer)
  - Use of modern high density IC technologies
  - Different basic electronics architectures to fit within limited area
- Significant sharing of deposited charge between neighbor cells in detector.
- Low detector capacitance (but significant capacitance to neighbors)
- Used for tracking in the highest particle rate parts of the detectors (close to interaction point) so detector and electronics must stand very high radiation levels (100Mrad).



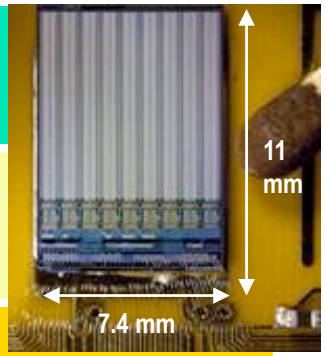






Pixel Readout architecture

Double column readout (ATLAS, CMS similar)
- 4 simultaneous tasks running



- Gray-coded time stamp distributed to all pixels
- when a pixel is hit, time is stored

- hits flagged to periphery with fast asynchronous scan
- time information and pixel address written into buffers shared by double column
- hit in pixel cleared

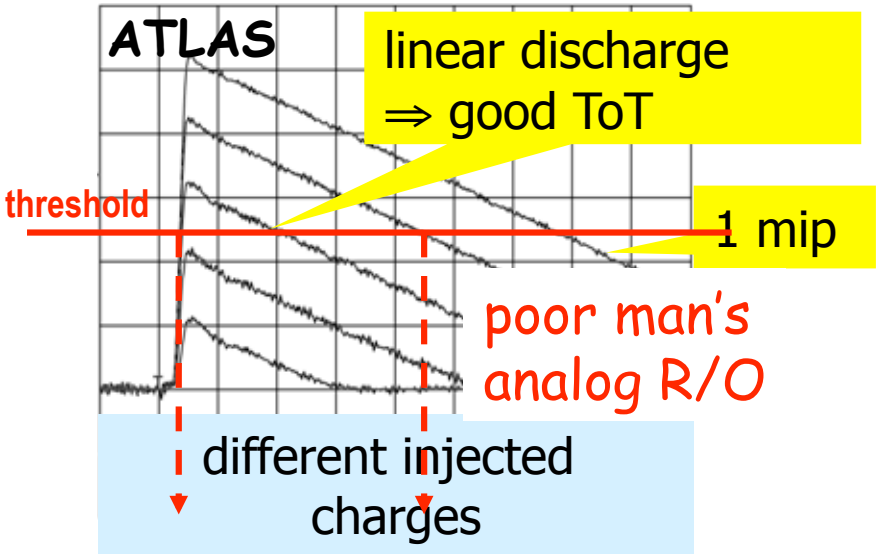
- if trigger arrives, hit time is compared to trigger, valid hits flagged, older hits deleted
- trigger queued in FIFO

- all valid hits serially read out

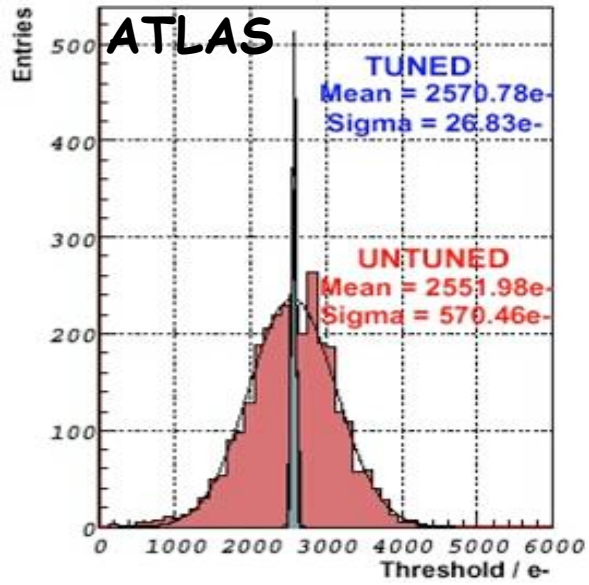
- explains why it is hard to use data in L1 trigger
- Both ATLAS and CMS preserve analogue signal information
  - ATLAS: Time over Threshold
  - CMS: analogue data saved in peripheral buffers

Hybrid pixels FE electronics

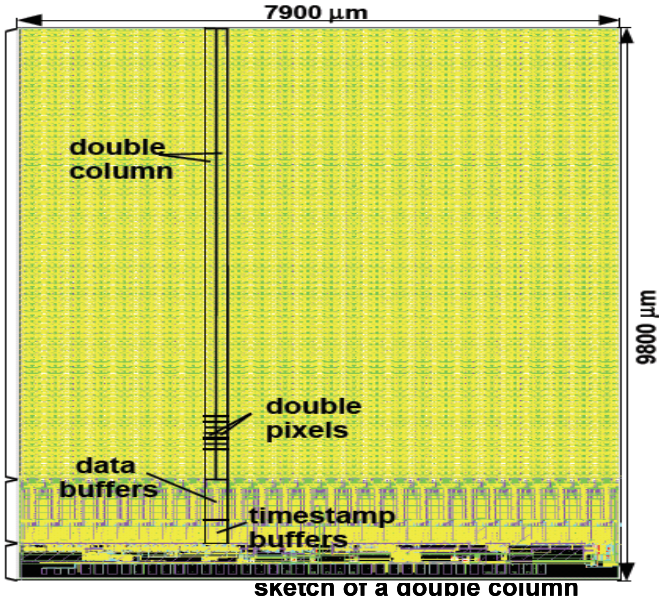
- Both ATLAS and CMS use 0.25µm CMS
- Preserve analogue signal information
  - using Time over Threshold (ATLAS)
    - noise ~160e on module
  - analogue data saved in peripheral buffers (CMS)



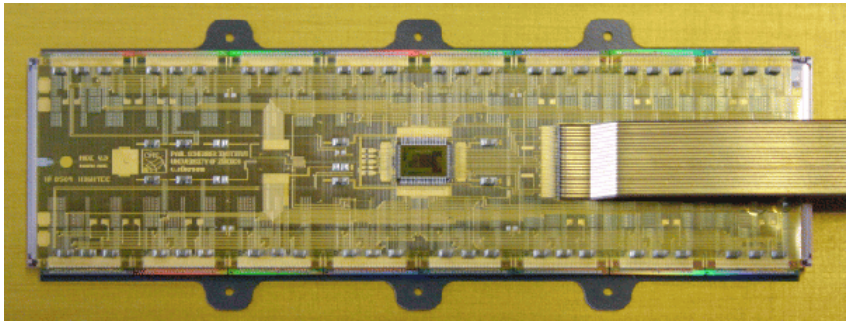
- Thresholds tuned using on-chip DACs
  - dispersion before tuning ~600e
  - after tuning <100e
- Crosstalk <1%

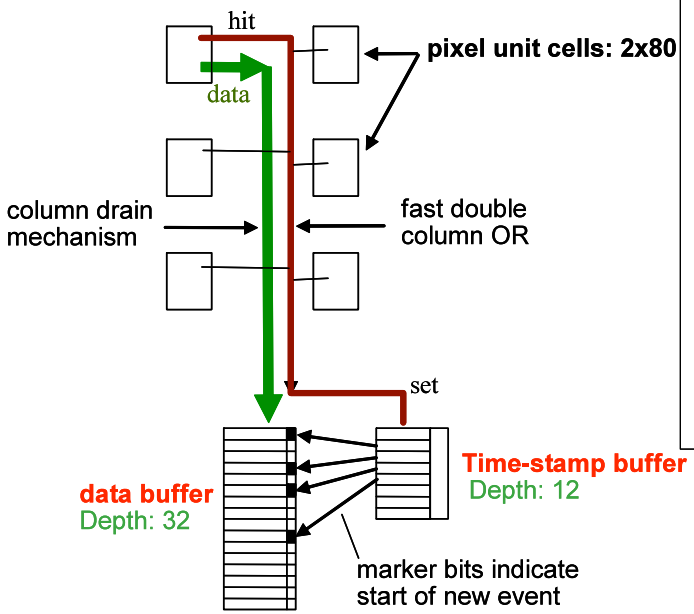


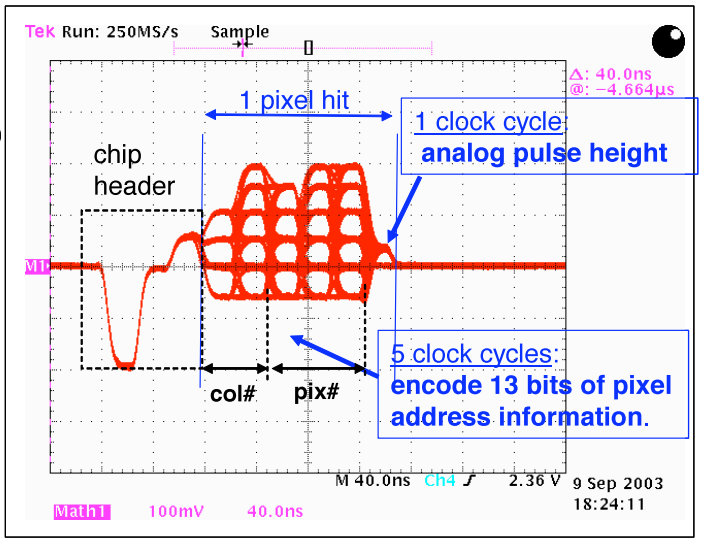
CMS pixel



sketch of a double column

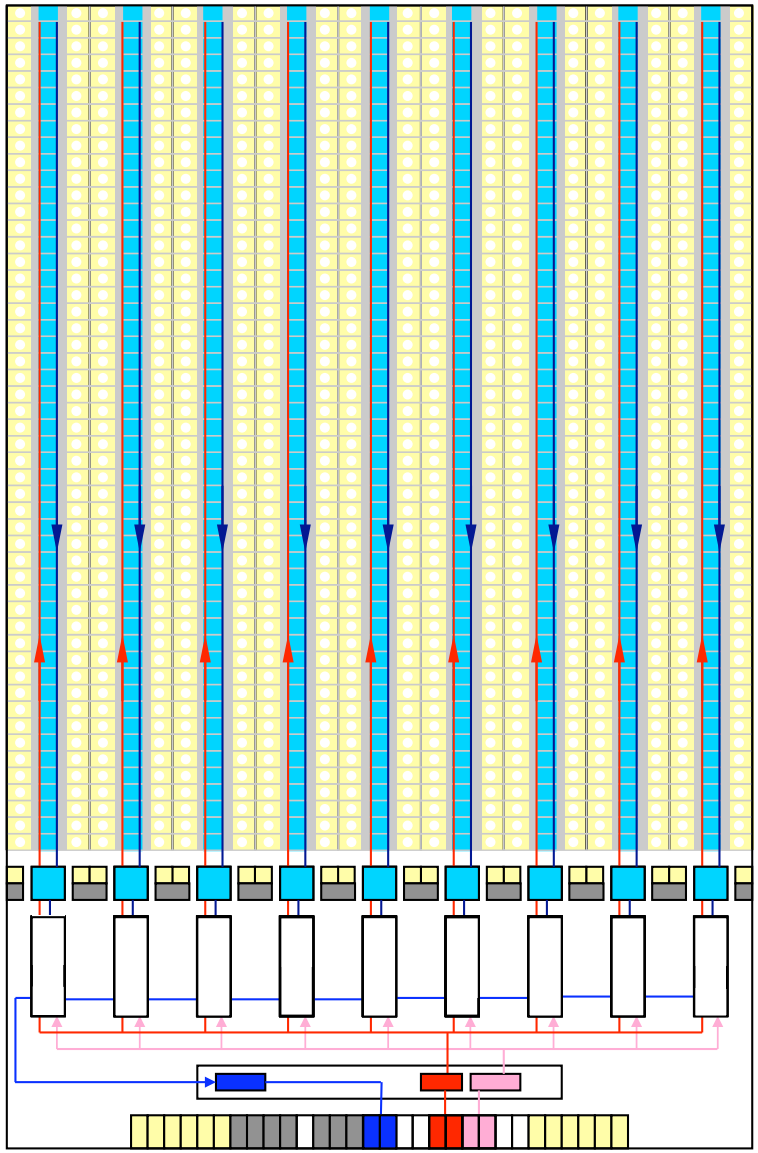






ATLAS Chip Architecture (animated)

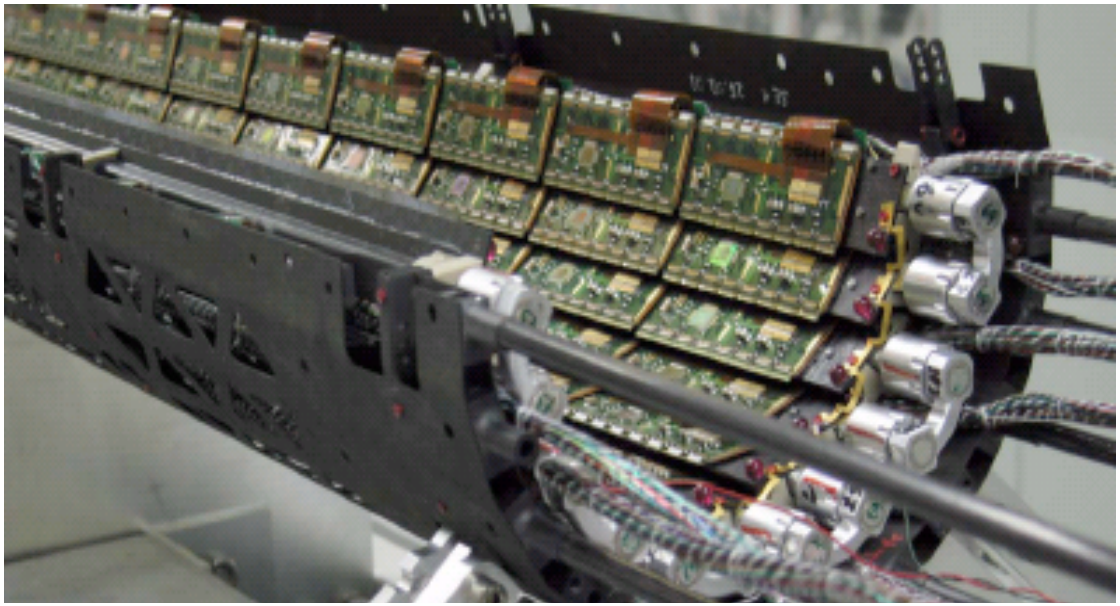
- 40 MHz Gray coded clock transmitted
- Pixel circuit detects sensor signal and generates hit information
- Hit data with time stamps are temporarily stored in end-of-column buffers
- The buffers monitor the age of hit data and delete them when no trigger coincidence occurs
- Hits having their time stamps coincident with L1 trigger are read out.

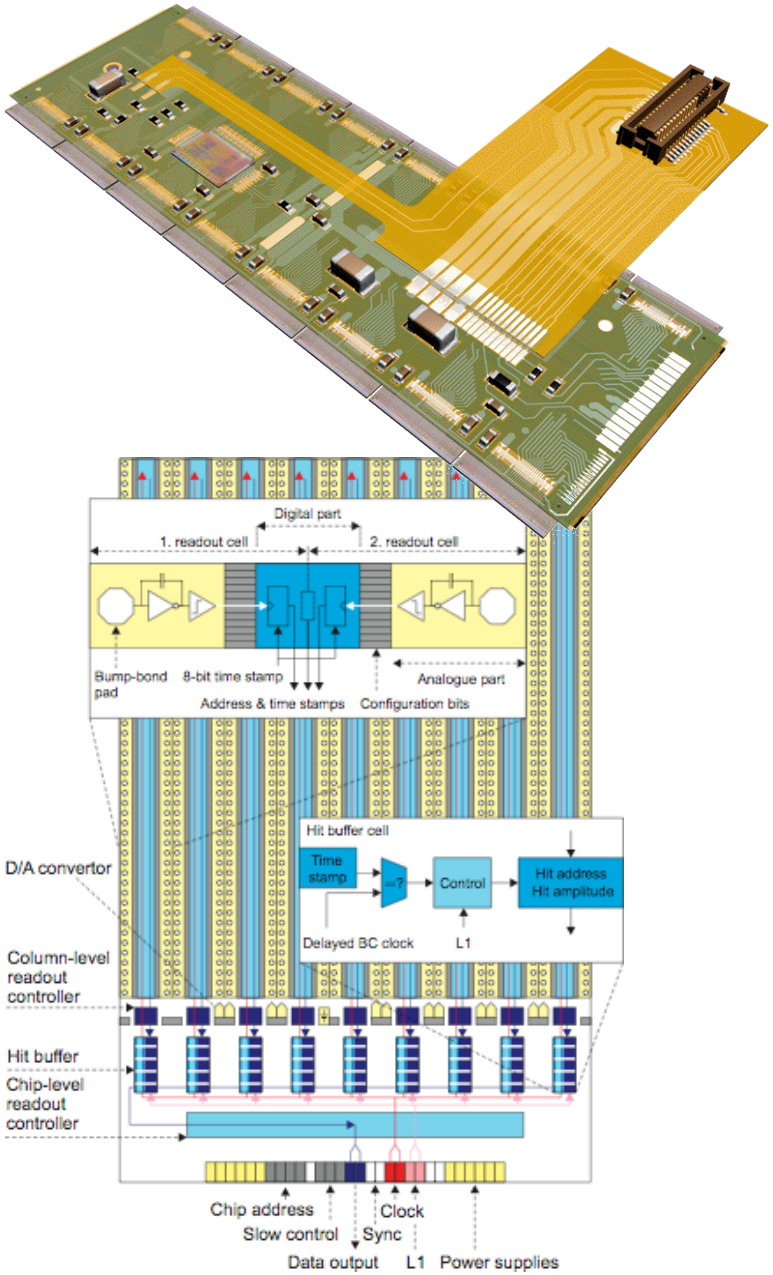


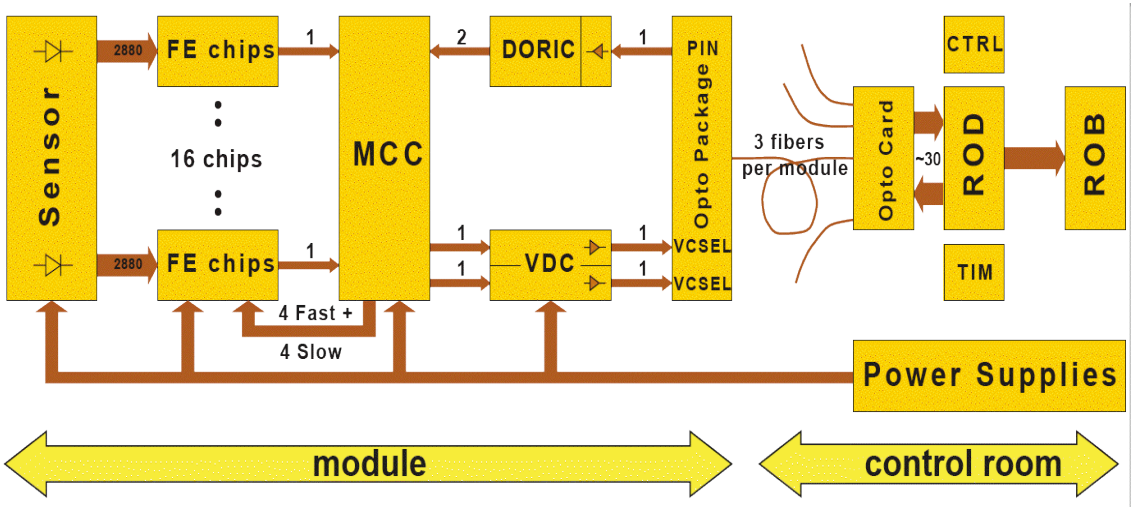
- Analogue circuits
- Digital readout circuits
- Registers used to store configuration bits
- Time information
- Trigger

from I. Peric

ATLAS pixel

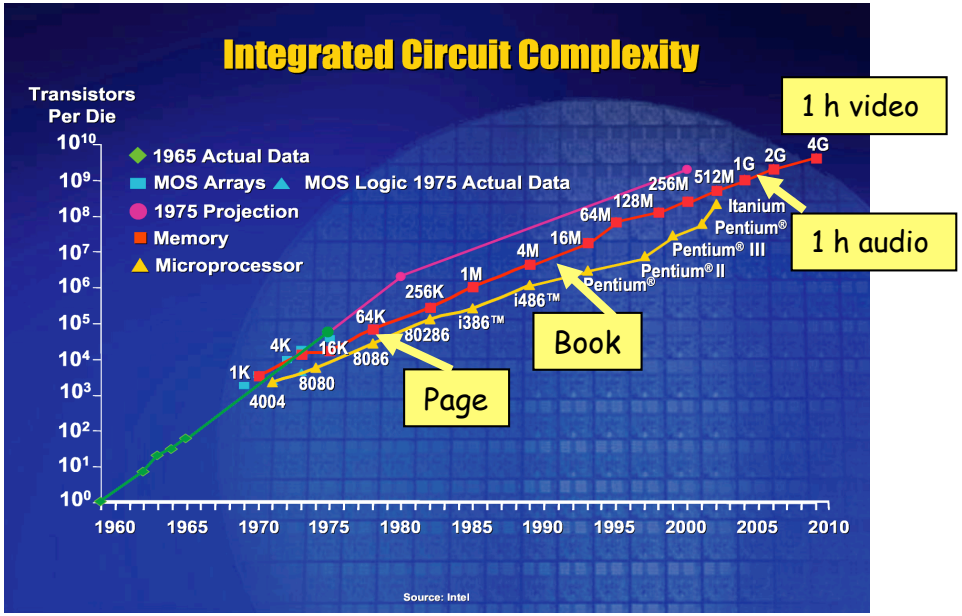


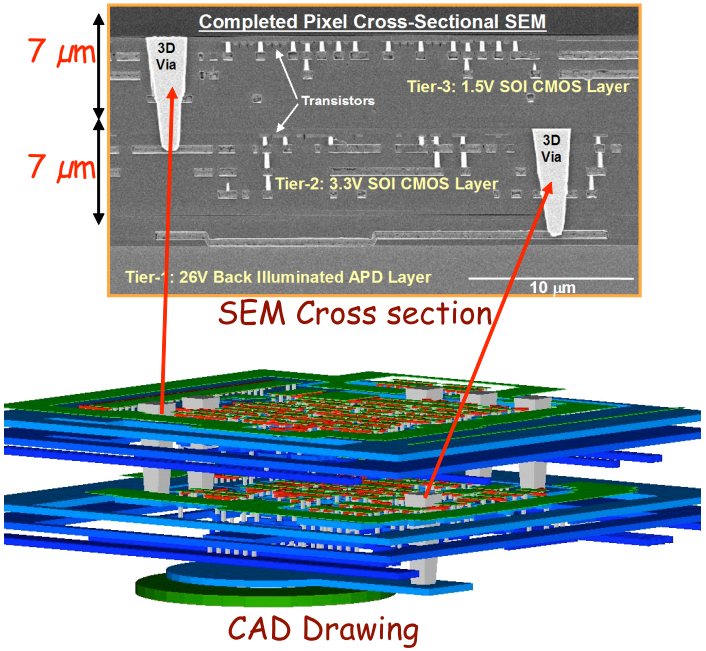

Digital part
1. readout cell
2. readout cell
Bump-bond pad
8-bit time stamp
Address & time stamps
Analogue part
Configuration bits
Hit buffer cell
D/A convertor
Time stamp
Control
Hit address
Hit amplitude
Delayed BC clock
L1
Column-level readout controller
Hit buffer
Chip-level readout controller
Chip address
Slow control
Sync
Clock
Data output
L1
Power supplies


Sensor
2880
FE chips
16 chips
2880
FE chips
1
MCC
2
DORIC
1
PIN
Opto Package
VCSEL
VCSEL
4 Fast +
4 Slow
VDC
3 fibers per module
Opto Card
~30
CTRL
ROD
TIM
ROB
Power Supplies
module
control room

Future

- The electronics of future detectors will be tightly integrated with the detectors themselves
  - MAPS
  - 3D packaging
  - High density hybrids and bump bonding
  - New and other ideas (SiPM, , ,)
- Radiation hardness of the electronics will remain a critical issue for hadron machines (but not so much for linear colliders)
- Power is a critical issue for detectors with all this electronics
  - Can become one of the major design criteria to keep the material of trackers at an acceptable level
- Increasing use of digital processing on detector (if power allows)
- High speed optical links will be needed in large quantity to get data out of the detector
- DAQ interfaces will benefit from the fast improvements in commercial electronics (e.g. FPGA's)





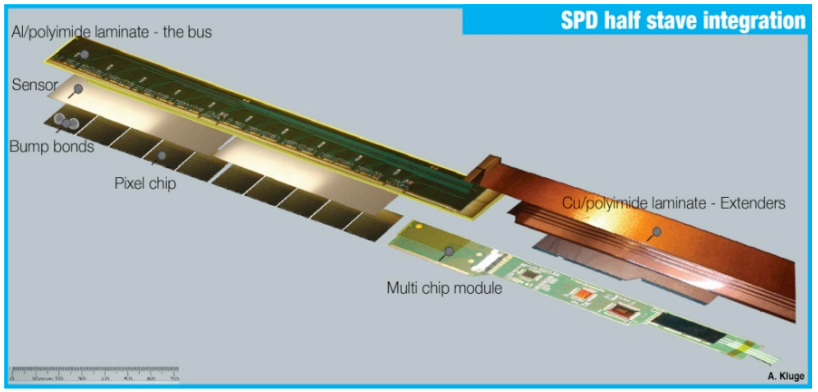
MORE SLIDES

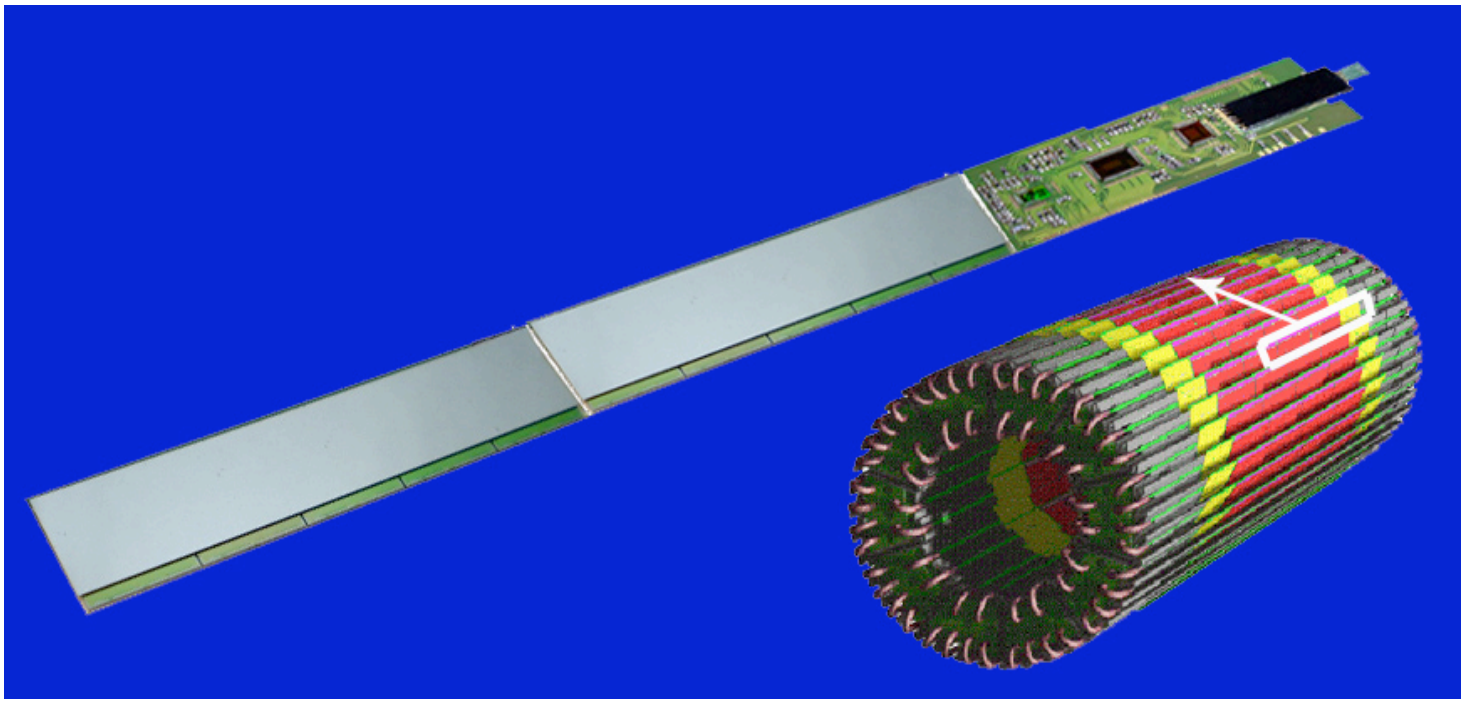
Electronics in HEP Experiments

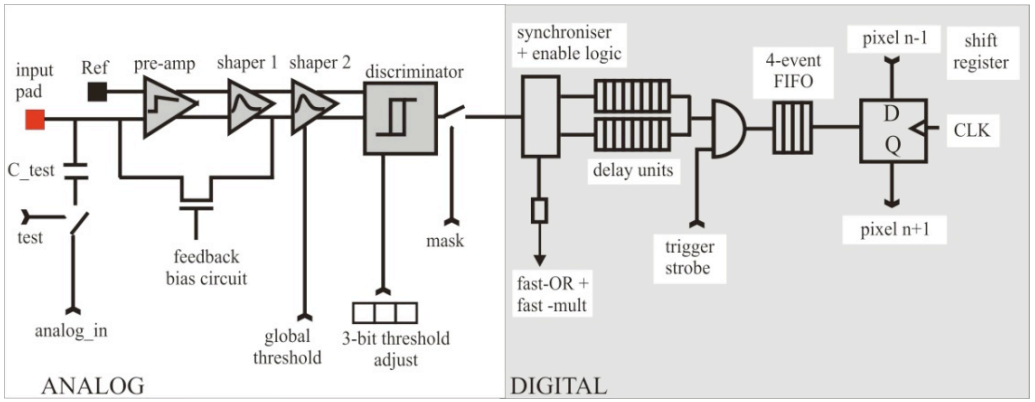
- Some slides are taken from CERN technical training ELEC 2005 mainly from Jeoff Hall and, to a lesser extent, from the CERN summer student lectures from Jorgen Christiansen, Christophe de la Taille, and Philippe Farthouat:
  - http://indico.cern.ch/categoryDisplay.py?categId=345
- Useful and more complete information can be found in the following sites:
  - CERN technical training ELEC 2005: http://indico.cern.ch/conferenceDisplay.py?confId=62928
  - LEB/LECC/TWEPP workshops from last 12 years: http://lhc-electronics-workshop.web.cern.ch/lhc%2Delectronics%2Dworkshop/
  - PH-ESE seminars: http://indico.cern.ch/categoryDisplay.py?categId=1591

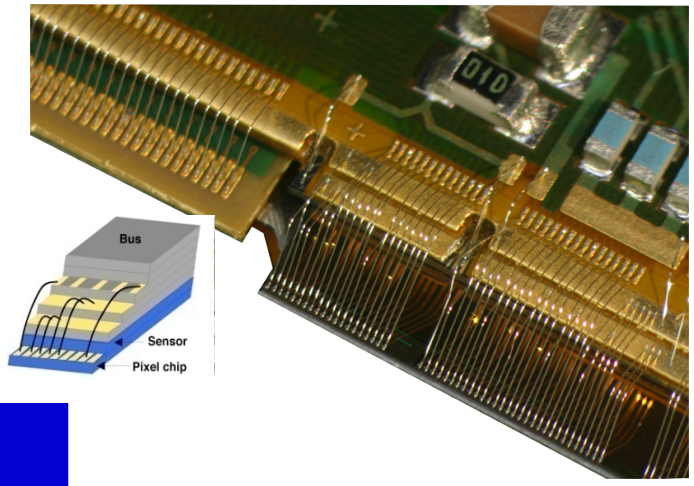
ALICE pixel

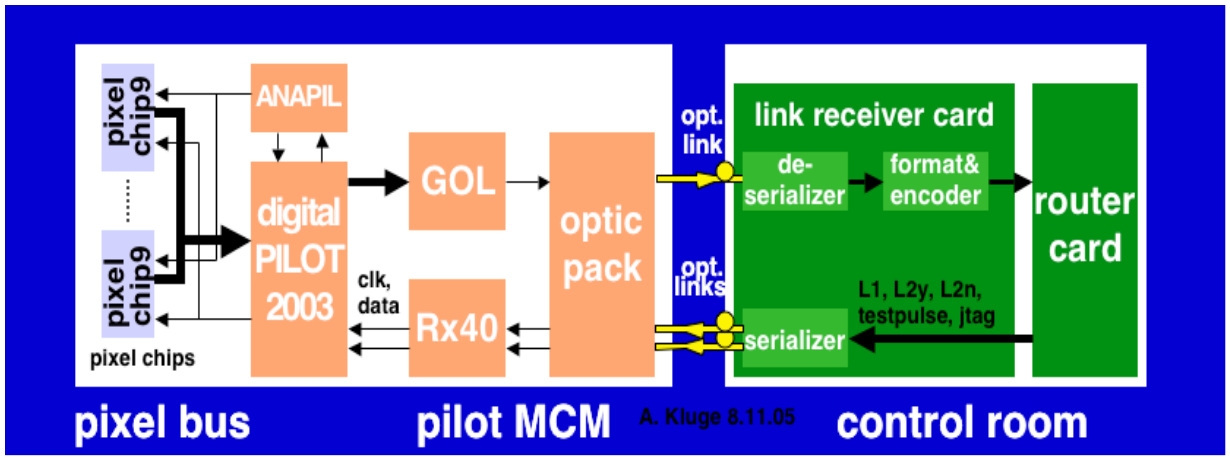
- 10M channels, 1200 pixel chips
- 120 detector modules
- Readout time: 256 μs
- Radiation: 250 krad
- Material: 1% X_0 per layer
- Power: 1kW

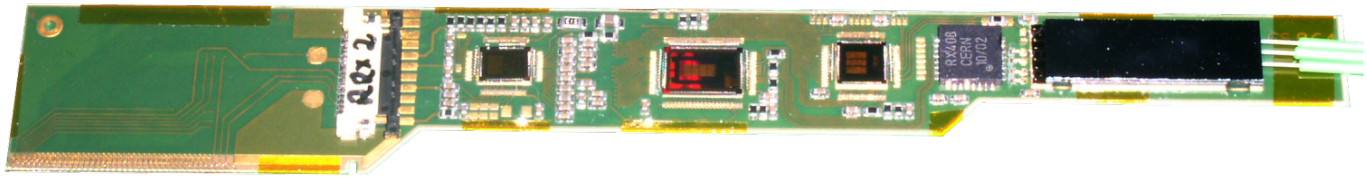





input pad
Ref
pre-amp
shaper 1
shaper 2
discriminator
C_test
test
feedback bias circuit
analog_in
global threshold
3-bit threshold adjust
mask
ANALOG
synchroniser + enable logic
delay units
4-event FIFO
pixel n-1
shift register
D
Q
CLK
pixel n+1
trigger strobe
fast-OR + fast -mult
DIGITAL

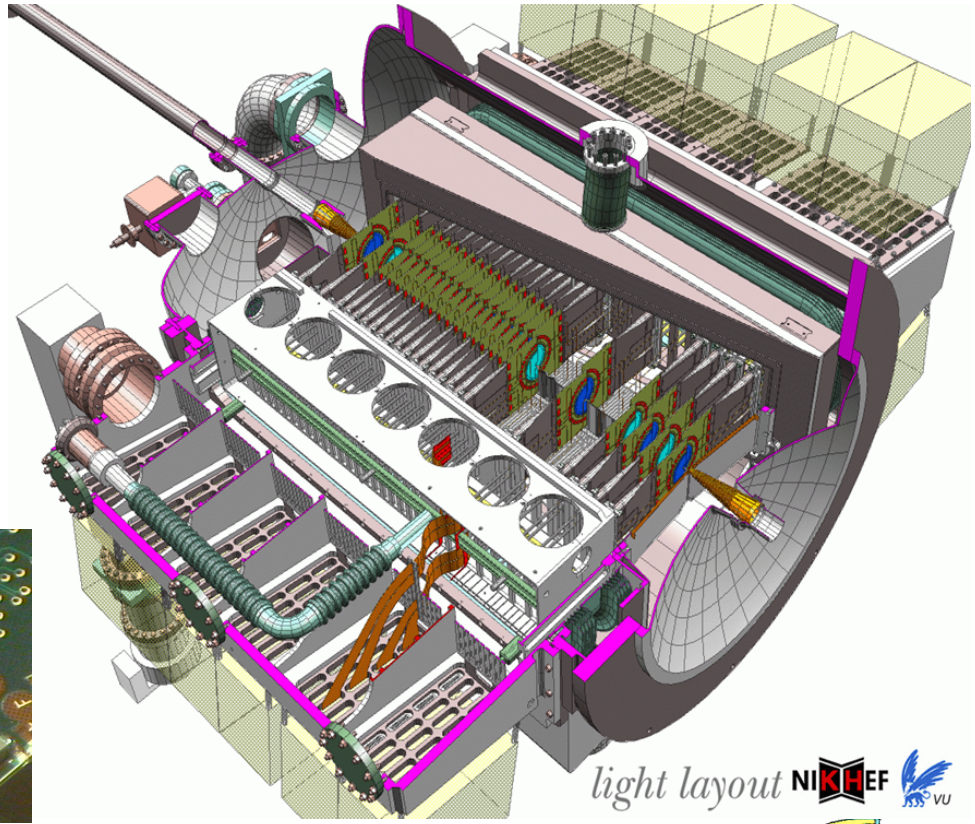

Bus
Sensor
Pixel chip

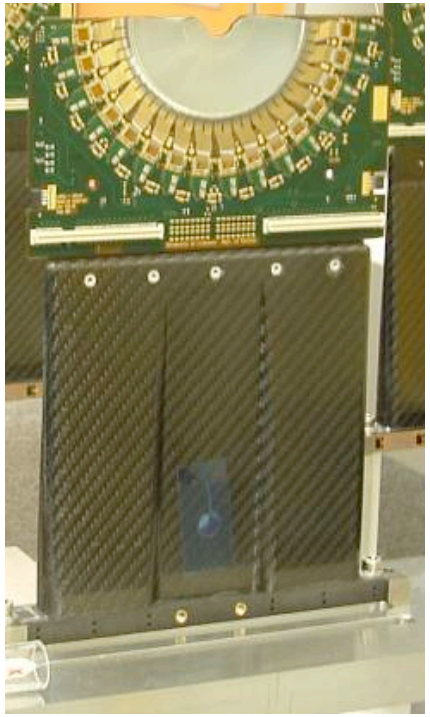

pixel chip9
pixel chip9
pixel chips
ANAPIL
digital PILOT 2003
clk, data
GOL
Rx40
optic pack
opt. link
opt. links
link receiver card
de-serializer
format& encoder
router card
L1, L2y, L2n, testpulse, jtag
serializer
pixel bus
pilot MCM
A. Kluge 8.11.05
control room

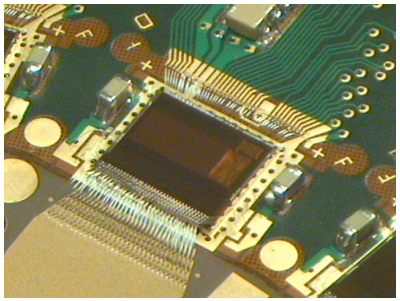


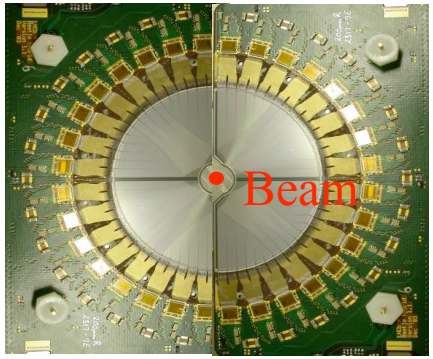
LHCb vertex

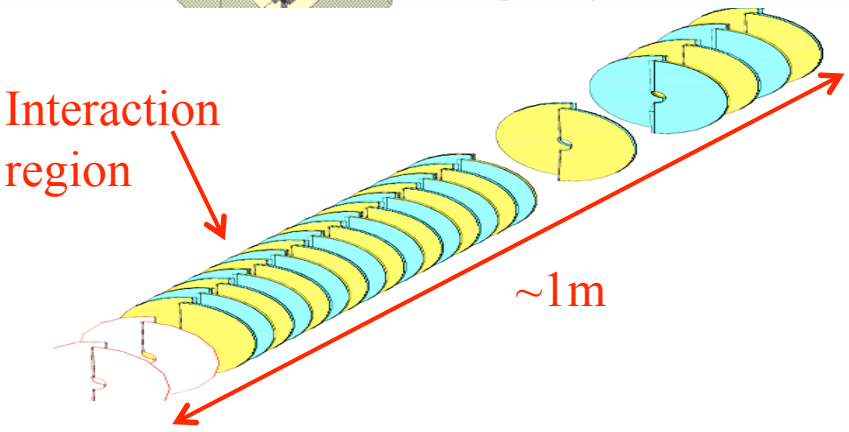
- 172k Channels
- Strips in R and φ projection (~10um vertex resolution)
- Located 1cm from beam
- Analog readout (via twisted pair cables over 60m)





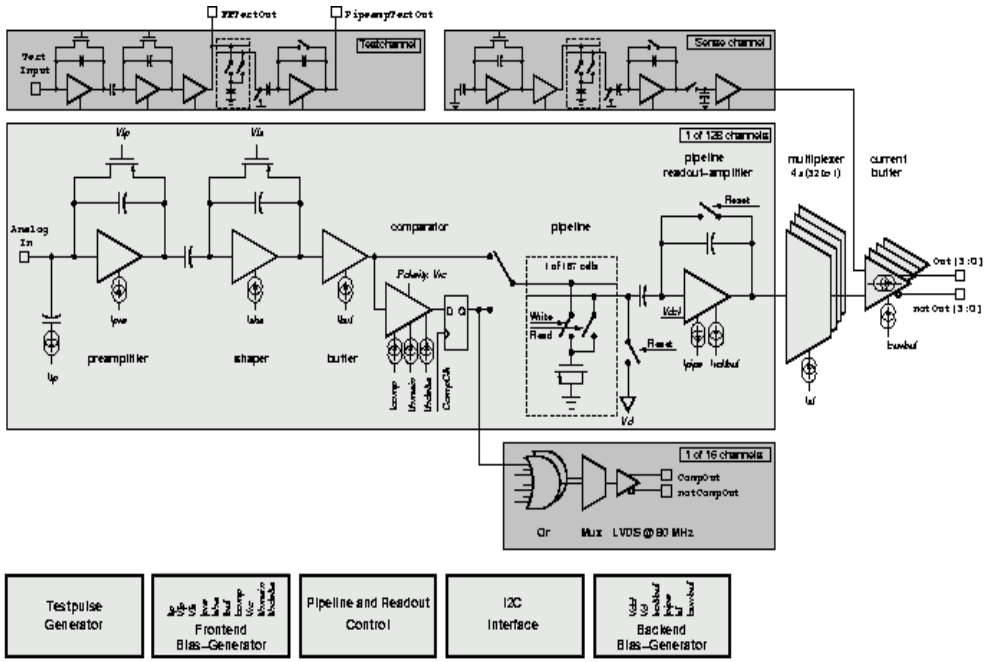


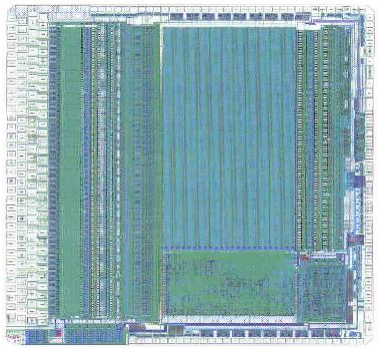


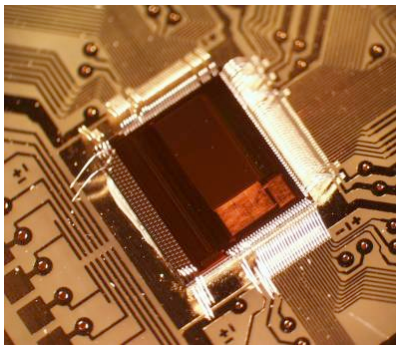


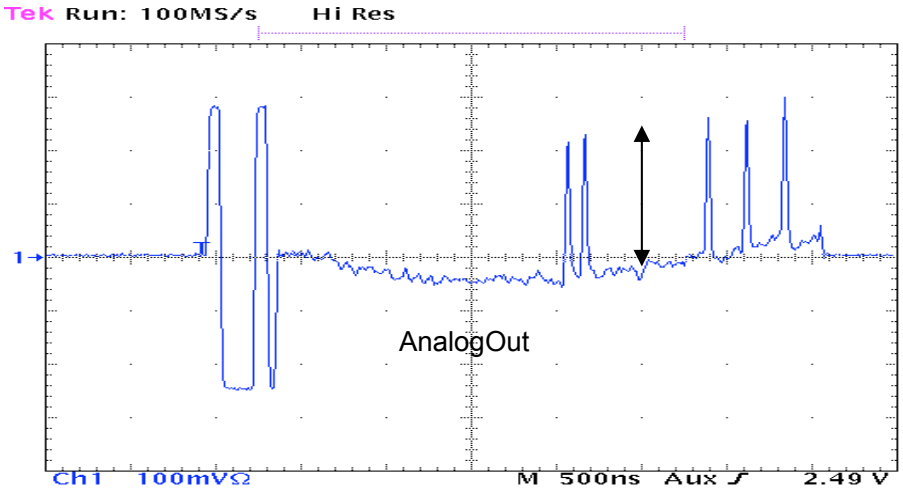
BEETLE

- Front-end chip of LHCb Vertex, trigger tracker, silicon tracker and pileup detectors.
  - 128 channels
  - Low noise preamp
  - Shaper with programmable shaping time
  - Analog memory for L0 latency and L0 derandomizer,
  - Analog readout at 1 MHz event rate over four analog differential links.
  - Discriminators for pileup (or of 4 ch.)
  - Radiation hard 0.25 um CMOS.
  - Triple redundant logic (SEU)
- Performance
  - Fully functional up to 100MHz
  - Excellent noise characteristics
    - ~540 e^- + 50e^-/pf
  - Temperature, voltage, and trigger tests performed
  - Extensive detector tests made
  - Radiation hard to above 10Mrad



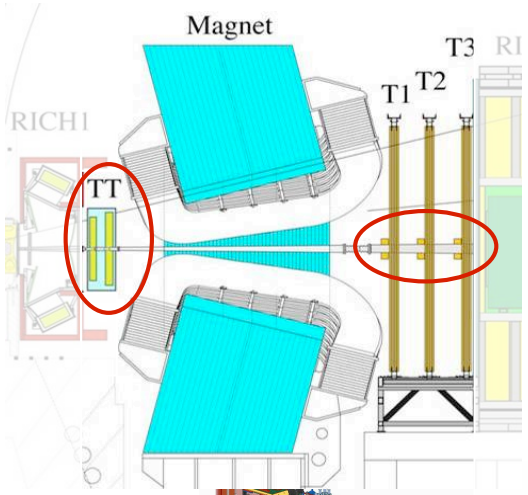


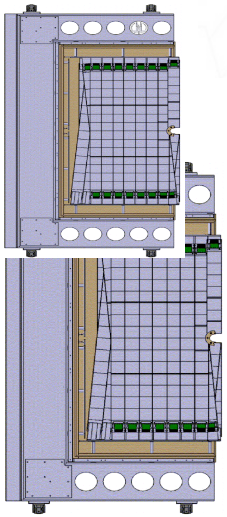


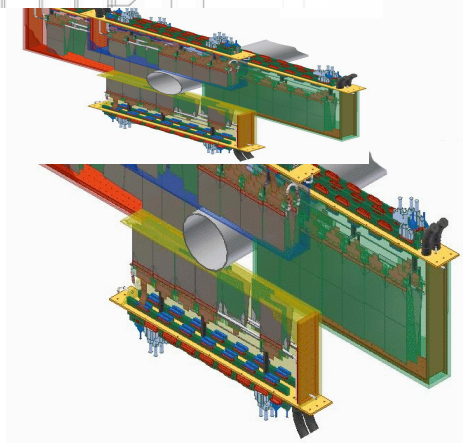


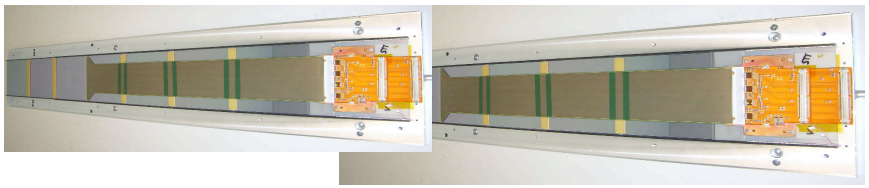
LHCb Silicon tracker

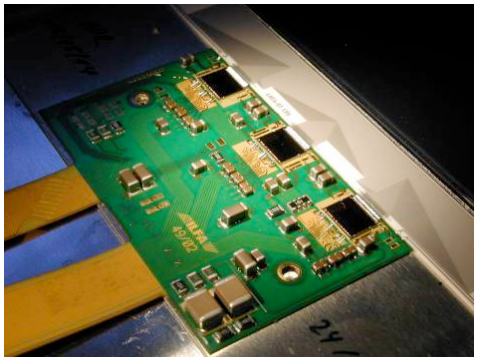
- 300k channels
- Silicon ladders of 2 – 4 silicon detectors chained to one electronics channel (relatively high capacitance)
- 600 Hybrids with 3 / 4 Beetle.
- Digitization on detector and digital optical links

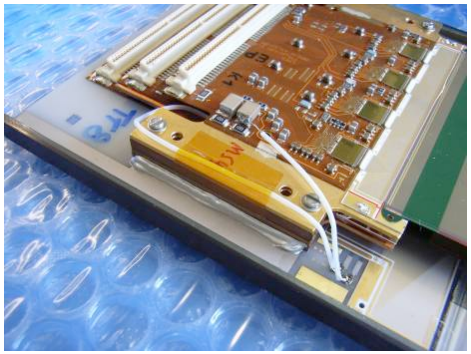






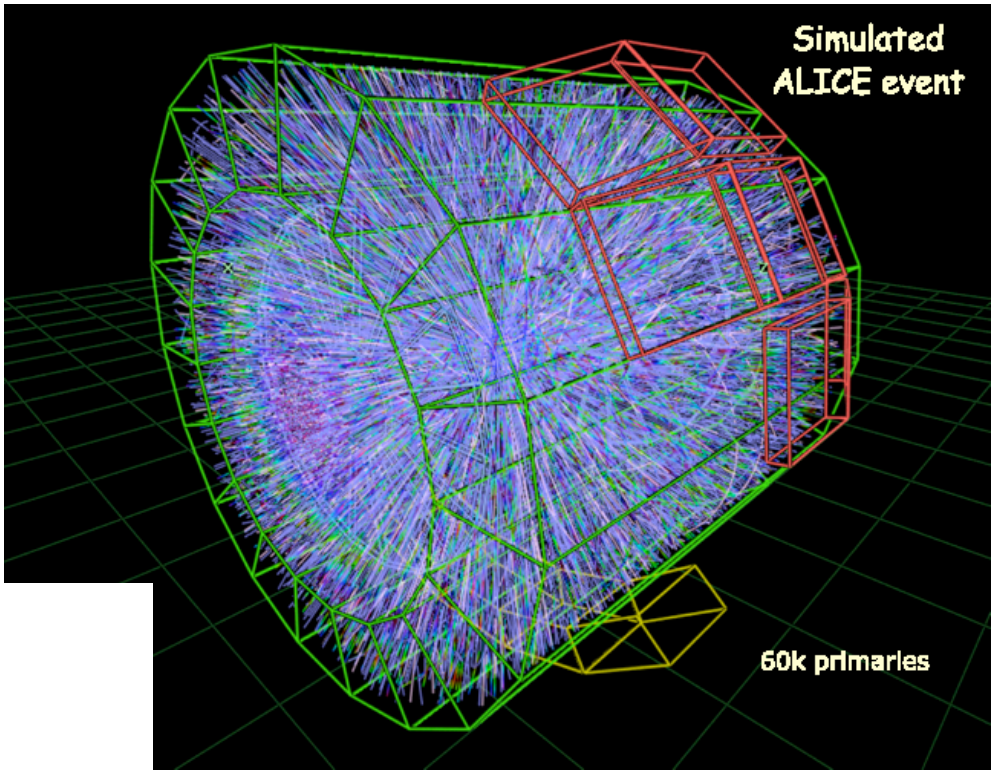


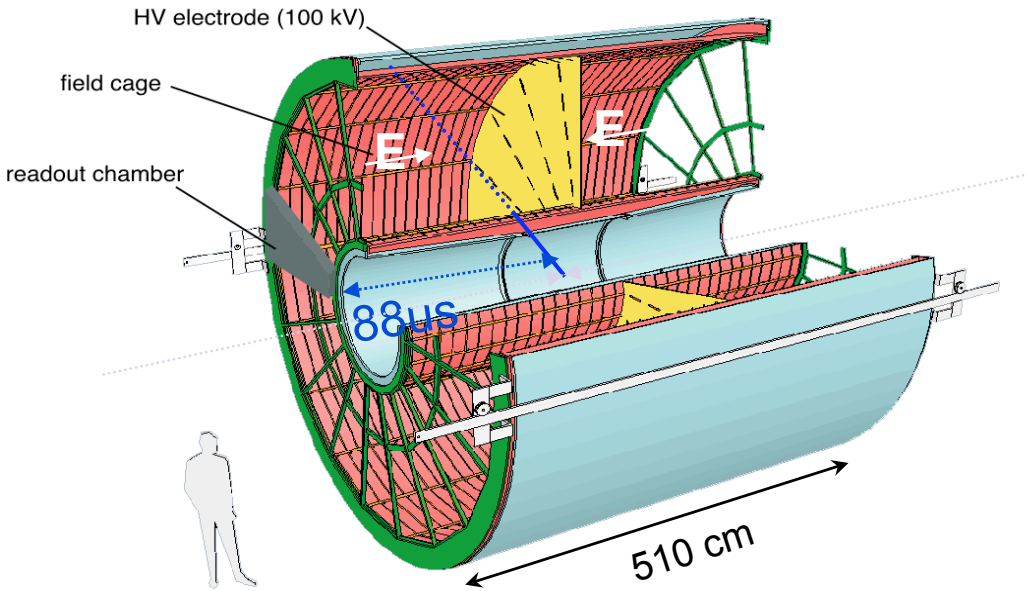


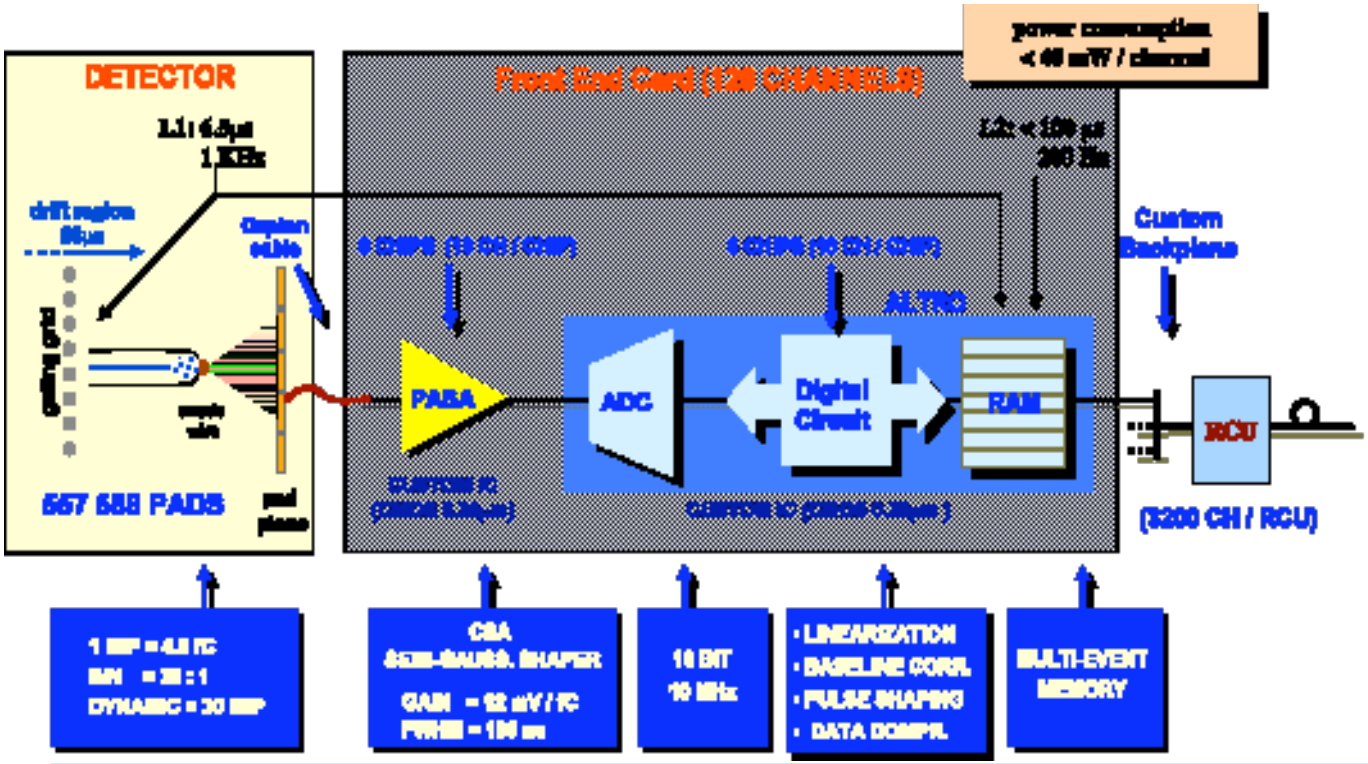


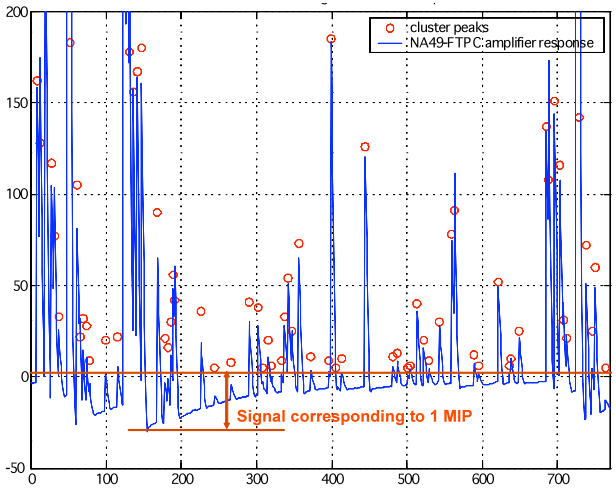
Alice TPC

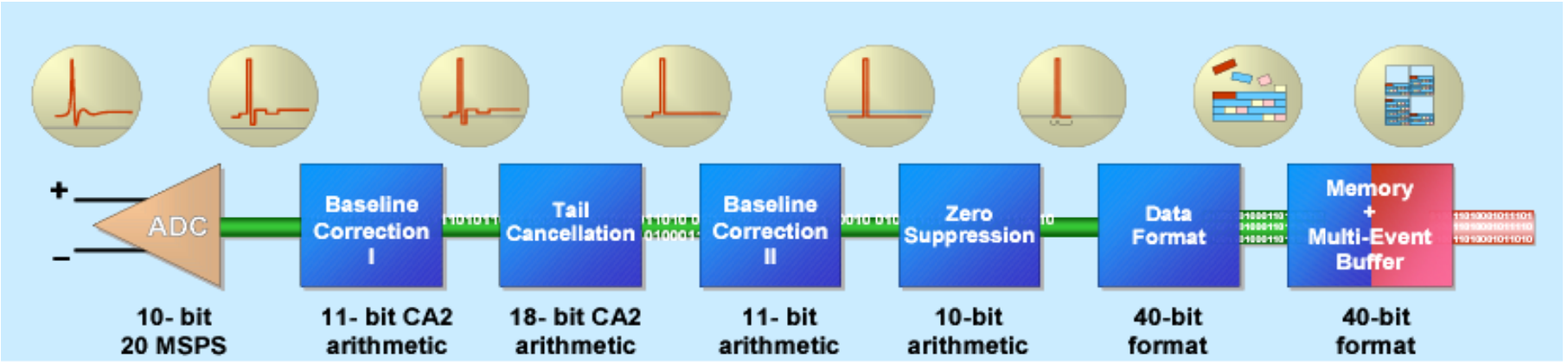
- Time projection chamber (long readout time)
- Main tracking/PID detector in ALICE
- Very high track density
- 558k pad channels
- Continuously sampled signal with on-detector DSP and zero-suppression





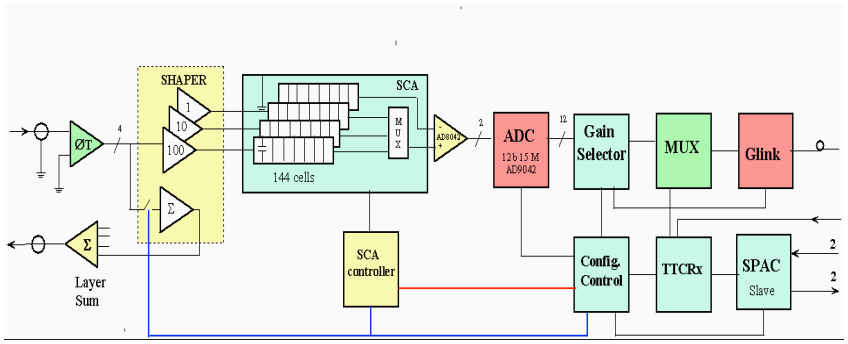

DETECTOR
Front End Card (128 CHANNELS)
power consumption
< 40 mW / channel
Custom
Backplane
PASA
ADC
Digital
Circuit
RAM
RCU
(3200 CH / RCU)
557 568 PADS
ALTRO
CBA
10 BIT
10 MHz
LINEARIZATION
BASELINE CORR.
PULSE SHAPING
DATA COMPR.
MULTI-EVENT
MEMORY

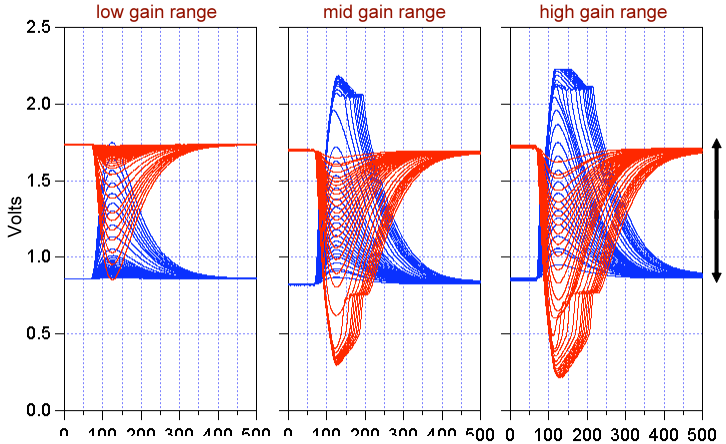

cluster peaks
NA49-FTPC amplifier response
Signal corresponding to 1 MIP
200
150
100
50
0
-50
0
100
200
300
400
500
600
700

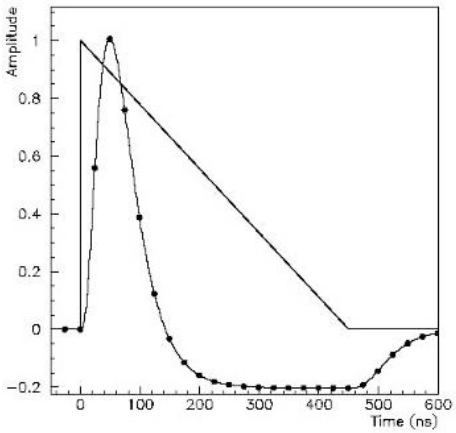

ADC
Baseline Correction I
Tail Cancellation
Baseline Correction II
Zero Suppression
Data Format
Memory + Multi-Event Buffer
10- bit 20 MSPS
11- bit CA2 arithmetic
18- bit CA2 arithmetic
11- bit arithmetic
10-bit arithmetic
40-bit format
40-bit format

Calorimeters

- Large dynamic range 12 – 16 bit
- Two common schemes to obtain required resolution and dynamic range
  - Multi gain architectures with ~3 signal paths. E.g. relative gains of 1, 4, 32. Use of single or multiple ADC's per channel
  - Non linear ADC with 10-12 bit resolution but covering 16 bit dynamic range
    - Has been tried on multiple occasions but turns out to be difficult to make in practice (calibration, assure constant nonlinear shape, etc.)
- Analog shaping typically done such that multiple samples per pulse are available
  - Lower bandwidth -> Lower noise in analog front-end
  - Digital filtering can remove pileup signals
  - Decreased quantization noise when multiple samples with real signal content are available
  - 4 – 8 samples per event including pre-samples to measure well baseline levels or pileup from previous signals.
- Zero-suppression with simple thresholding normally not applicable as this will give reduced energy resolution (halo of small signals around cell with major signal).
  - Zero-suppression with neighbor information
  - Data compression instead of zero-suppression
- Limited integration needed as Calorimeter cells normally several centimeters wide
  - Exception for new class of tracking calorimeters under development for ILC, CLIC, etc.

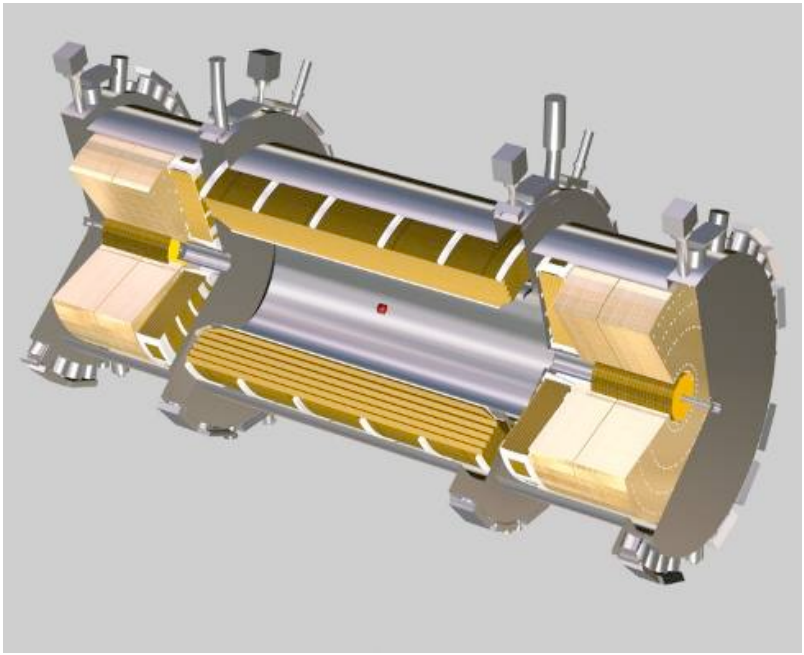


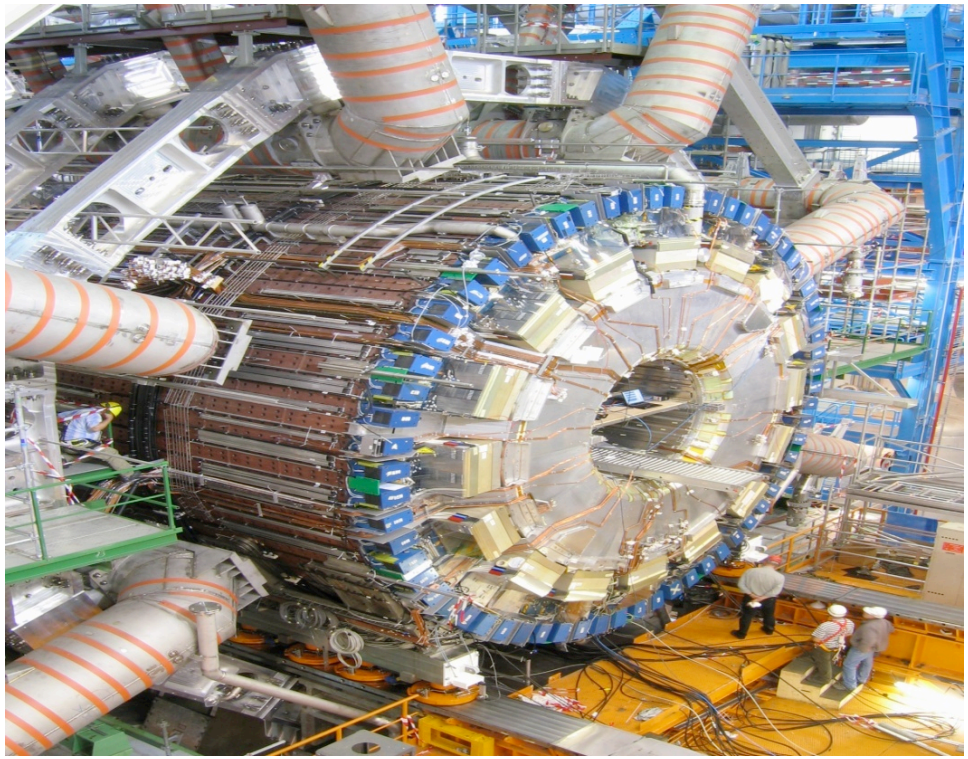


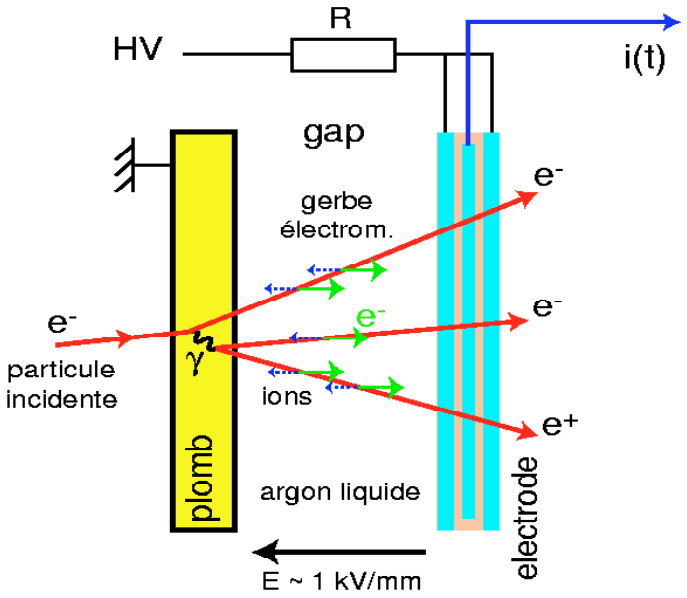


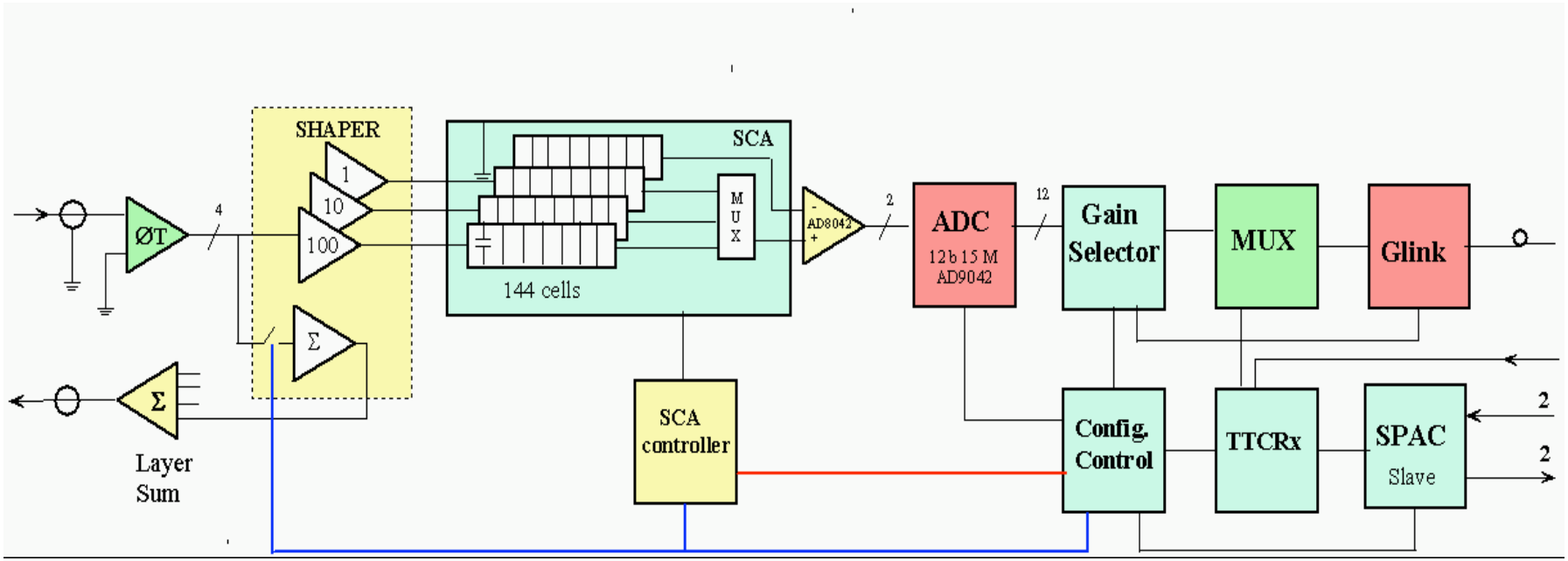
ATLAS Ecal

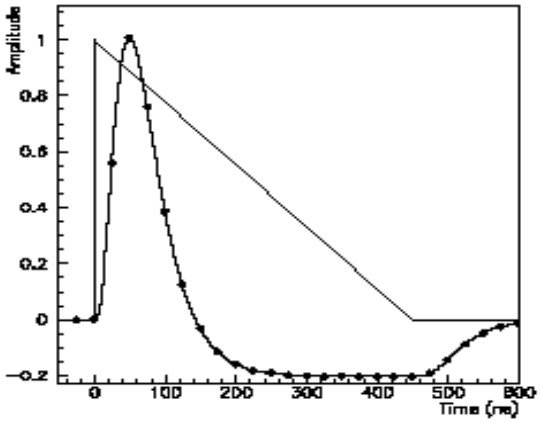
- 200k Channels
- 3 gain sub-channels
- Analog buffers
- 12 bit ADC

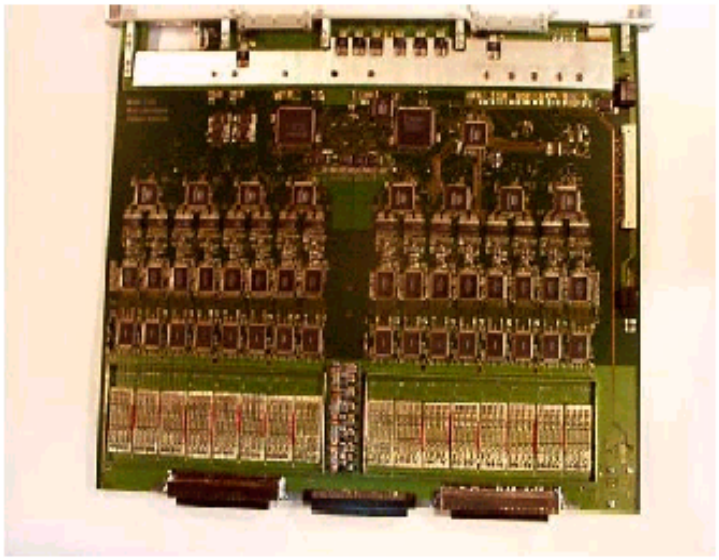






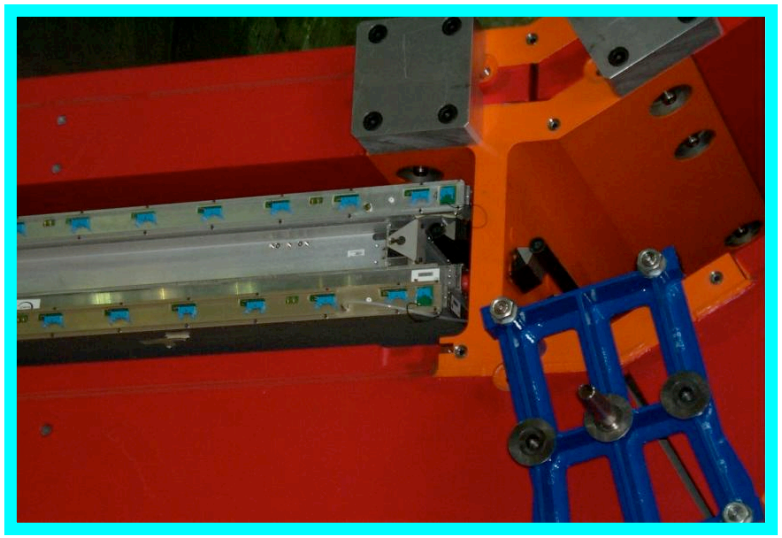

SHAPER
SCA
1
10
100
ØT
4
M
U
X
AD8042
2
ADC
12 b 15 M
AD9042
12
Gain
Selector
MUX
Glink
144 cells
Σ
Σ
Layer
Sum
SCA
controller
Config.
Control
TTCRx
SPAC
Slave
2
2

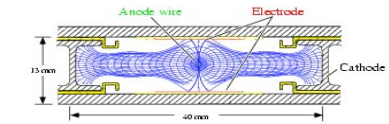

Amplitude
1
0.8
0.6
0.4
0.2
0
-0.2
0
100
200
300
400
500
600
Time (ns)



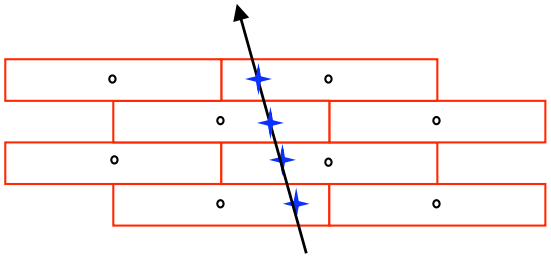
CMS muon

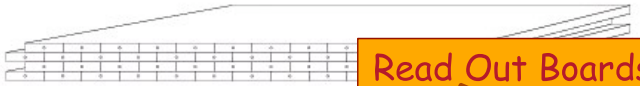
- 172k drift tubes
- 450ns drift time, Overlapping triggers
- ASDBLR and TDC

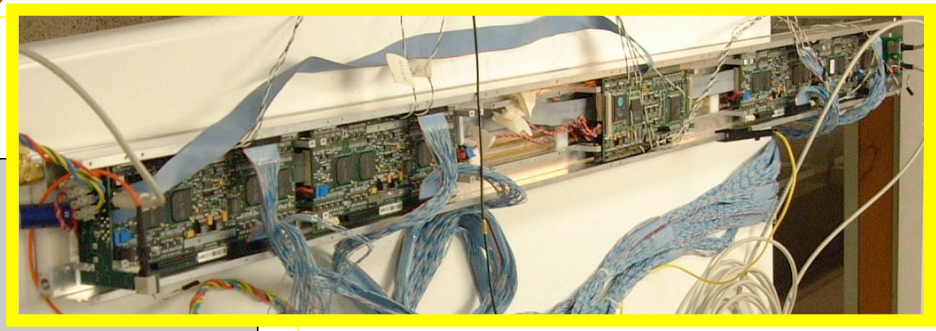


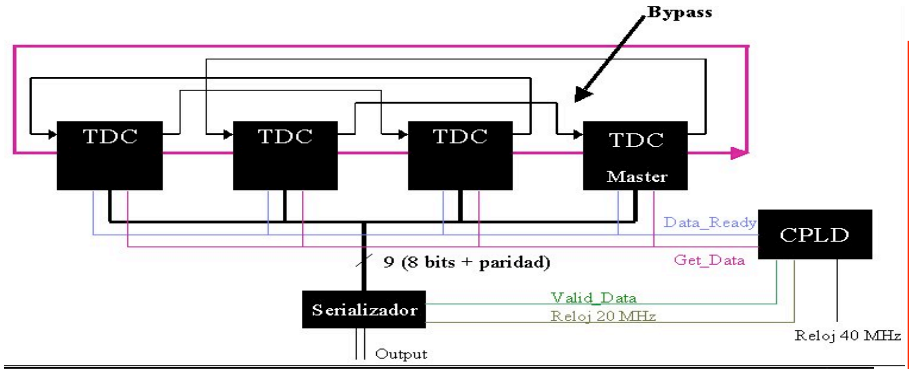


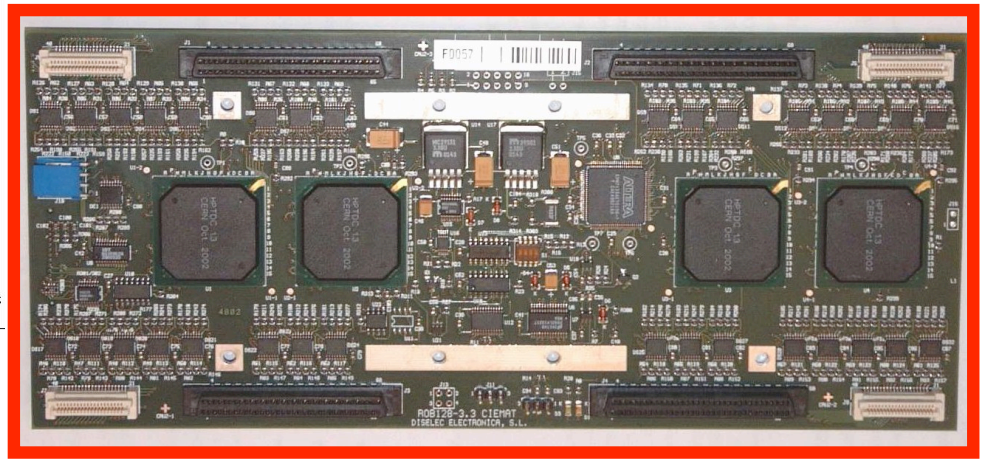
4 Layers = 1 SuperLayer (SL)

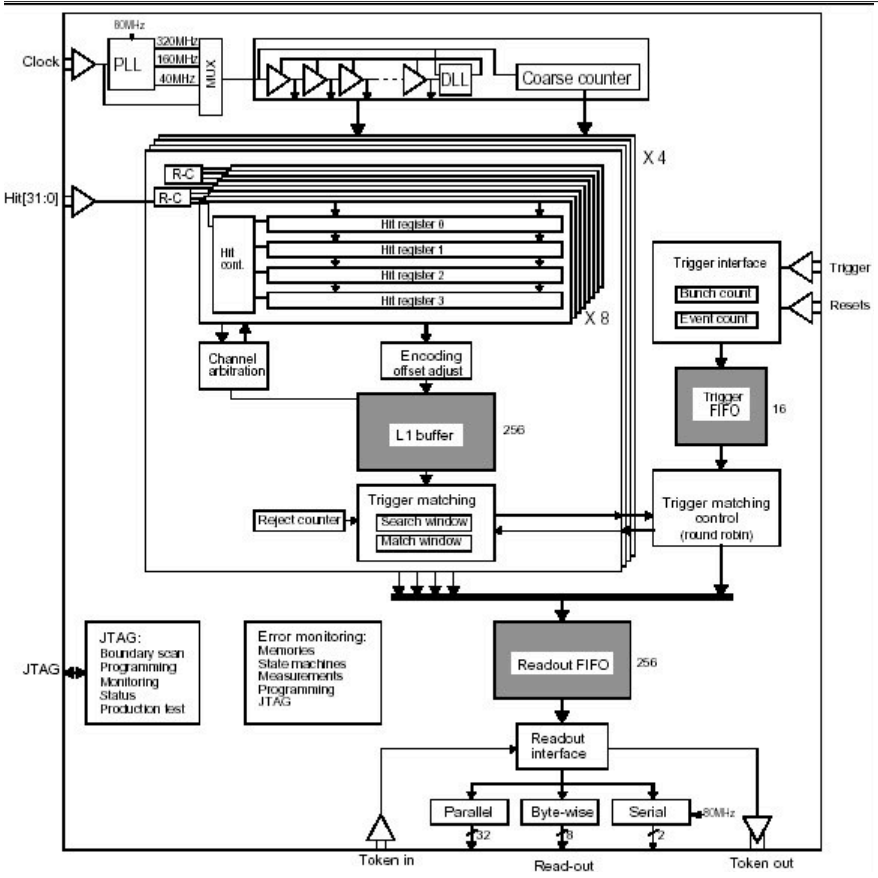


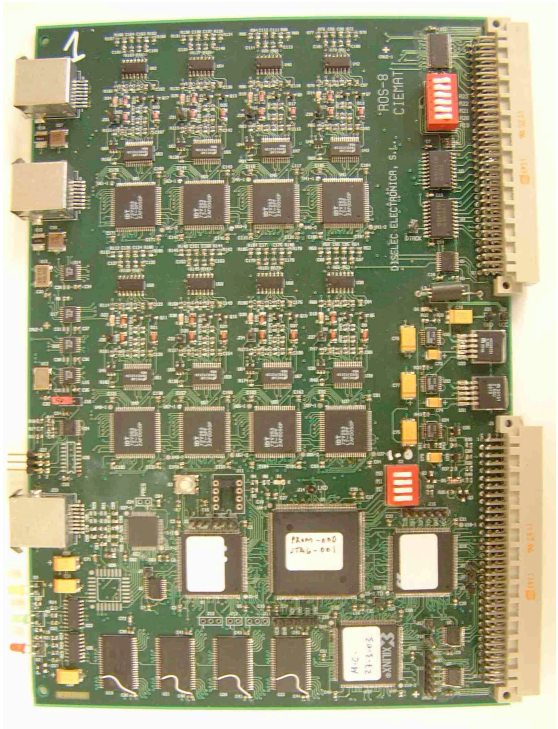





Bypass
TDC
TDC
TDC
TDC
Master
Data_Ready
CPLD
9 (8 bits + paridad)
Get_Data
Serializador
Valid_Data
Reloj 20 MHz
Reloj 40 MHz
Output

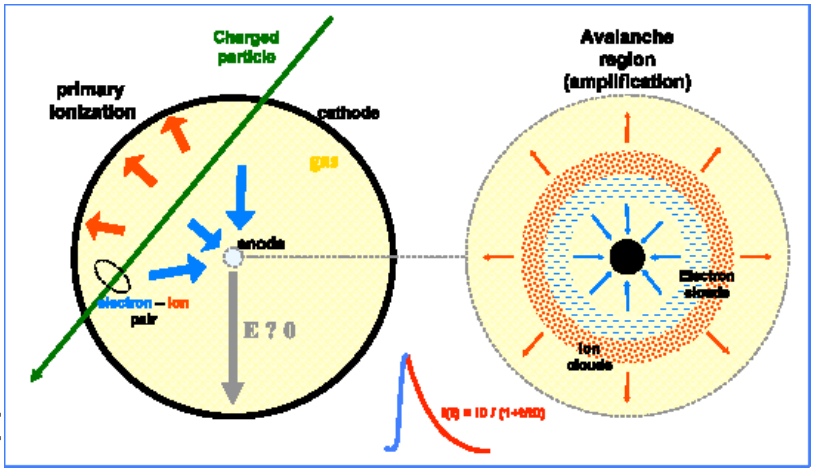


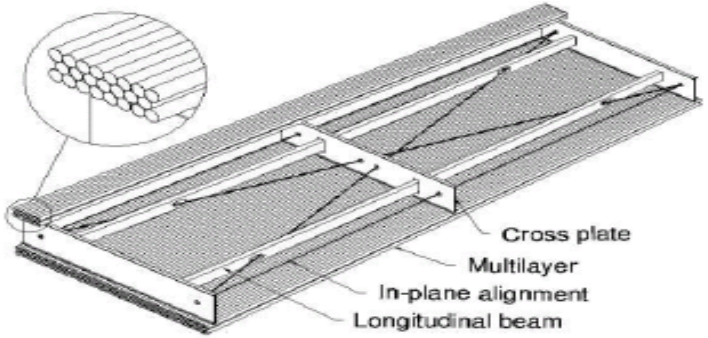

80MHz
Clock
PLL
320MHz
160MHz
40MHz
MUX
DLL
Coarse counter
X 4
R-C
R-C
Hit[31:0]
Hit cont.
Hit register 0
Hit register 1
Hit register 2
Hit register 3
X 8
Trigger interface
Bunch count
Event count
Trigger
Resets
Channel arbitration
Encoding offset adjust
Trigger FIFO
16
L1 buffer
256
Trigger matching
Search window
Match window
Reject counter
Trigger matching control (round robin)
JTAG
JTAG:
Boundary scan
Programming
Monitoring
Status
Production test
Error monitoring:
Memories
State machines
Measurements
Programming
JTAG
Readout FIFO
256
Readout interface
Parallel
Byte-wise
Serial
80MHz
32
8
2
Token in
Read-out
Token out

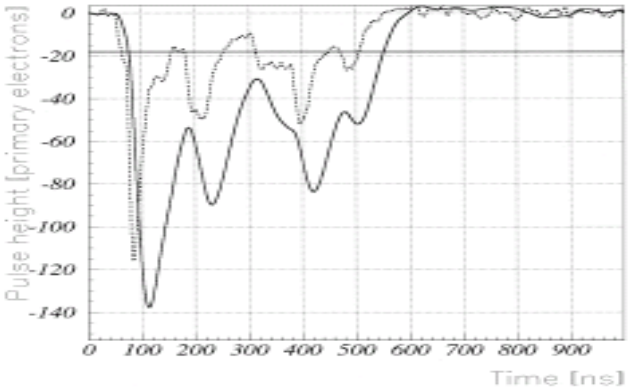


Drift tubes

- Used for tracking where hit rates are limited (but can be several MHz)
- Limited integration of electronics needed as channel density given by size of tubes (0.5 – 5 cm)
- ASDBLR and TDC with data buffering
- As drift tubes can be relatively long (several meters) the preamplifier must terminate the signal propagation with the characteristic impedance of the "coax" tube.
  - Otherwise multiple reflections will occur
  - Far end of tube should also be terminated but resistive termination will give some noise increase (signal reflections can though be a worse problem)
- Ion tail to be removed in dedicated filtering
- Signal consists of multiple clusters from primary ionizations
- Maximum drift time can be longer that maximum spacing between triggers
  - Requires special logic to allow detected hits to be assigned to multiple events for readout

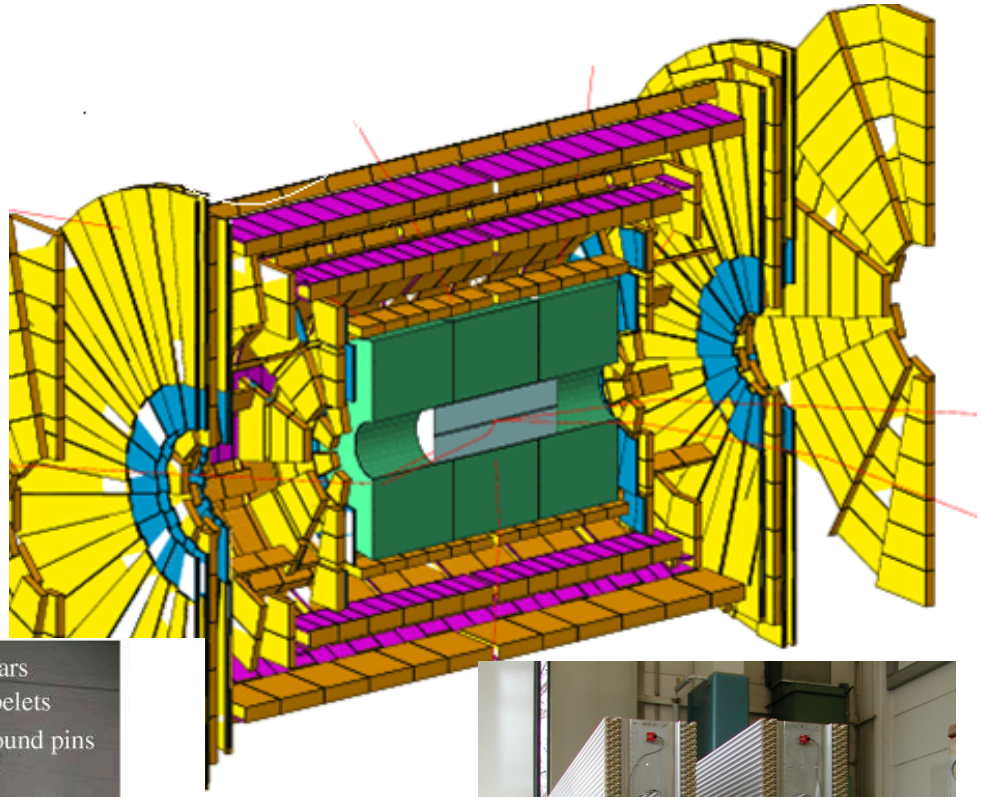


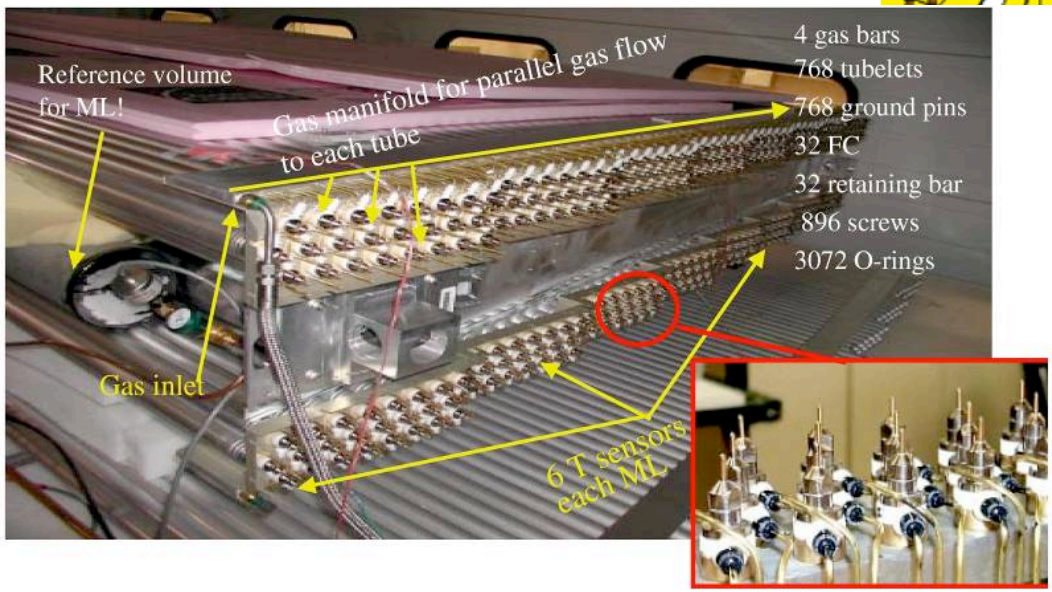


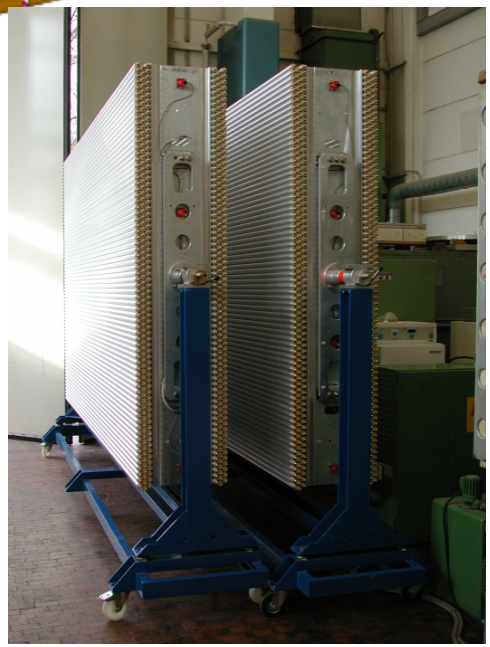


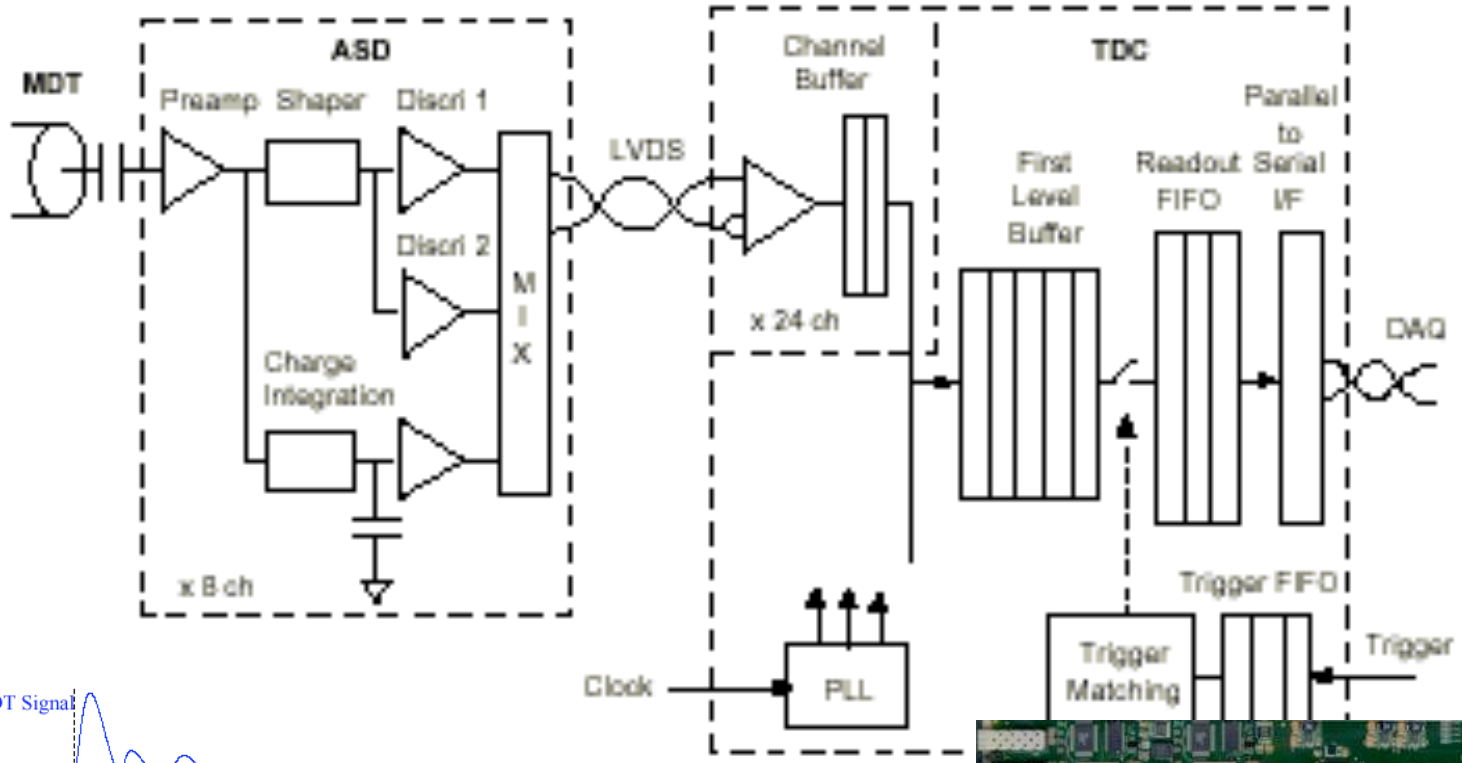
ATLAS MDT

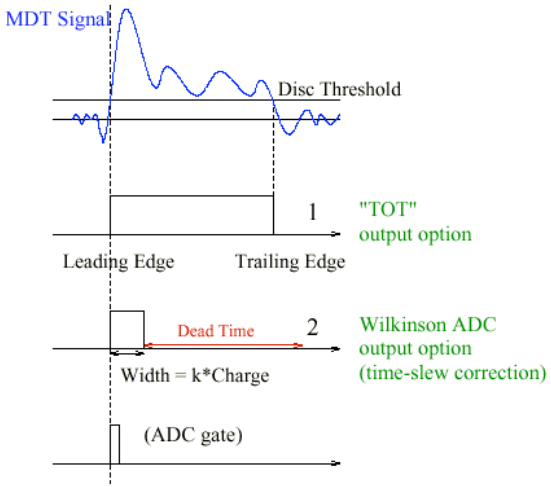
- 370k Channels
- 3 m long drift tubes
- Covers 5500m^2
- 500ns drift time





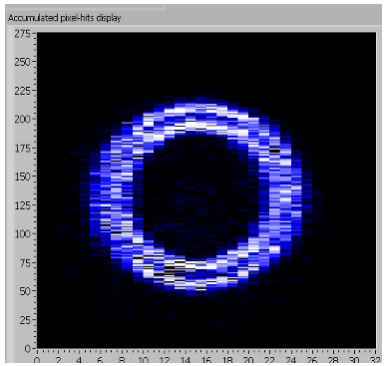


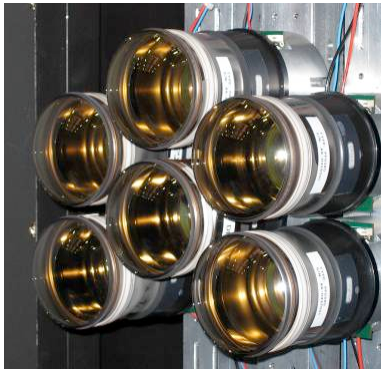

MDT
ASD
Preamp
Shaper
Discri 1
Discri 2
Charge Integration
M I X
x 8 ch
LVDS
Channel Buffer
x 24 ch
TDC
First Level Buffer
Readout FIFO
Parallel to Serial I/F
DAQ
Trigger FIFO
Trigger Matching
Trigger
Clock
PLL

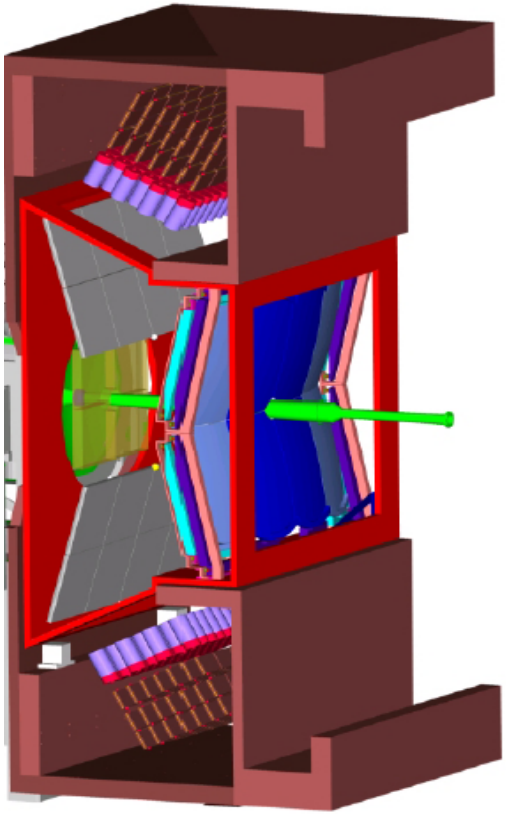

MDT Signal
Disc Threshold
1
"TOT"
output option
Leading Edge
Trailing Edge
Dead Time
2
Wilkinson ADC
output option
(time-slew correction)
Width = k*Charge
(ADC gate)

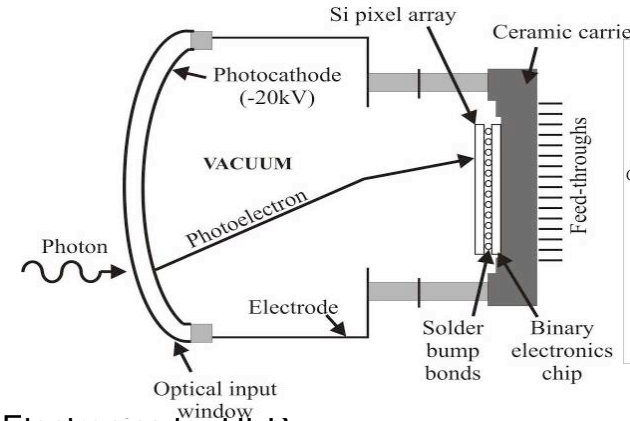
LHCb RICH

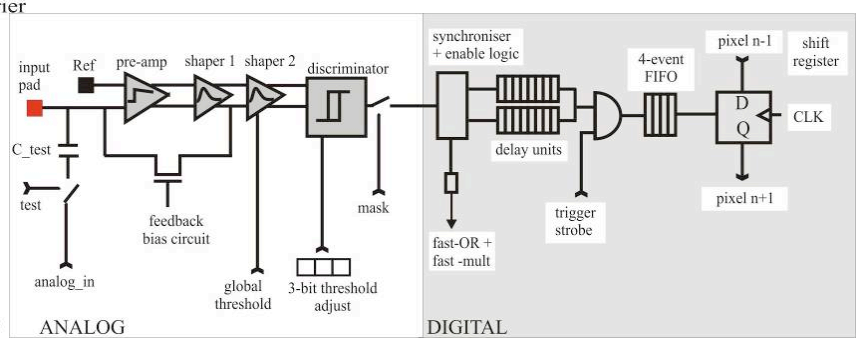
- Two RICH detectors for particle identification
- Based on 500 Hybrid Photon Detectors
- Each HPD vacuum tube contains a binary silicon pixel detector (1024 pixels)
  - Common development with ALICE
  - Does not have a L0 pipeline but a 16 hit buffer with time tags
- Local front-end card based on antifuse FPGA.
- Optical links to dedicated DAQ interface board

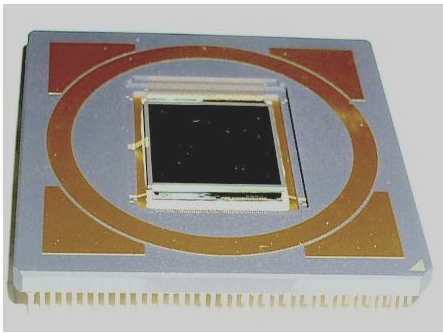






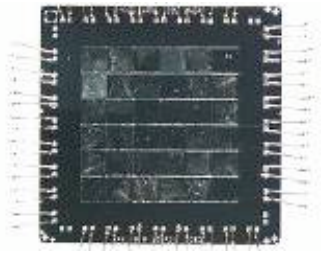






Detector(s)

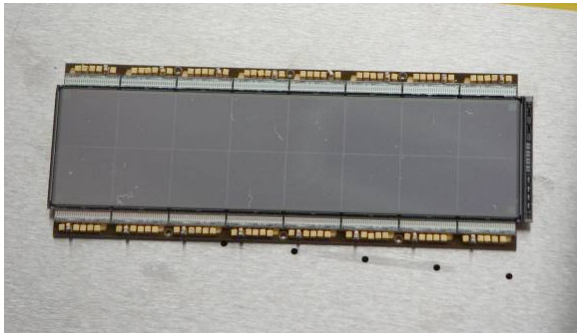
- A large variety



6x6 pixels,4x4 mm^2

PMT for Antares

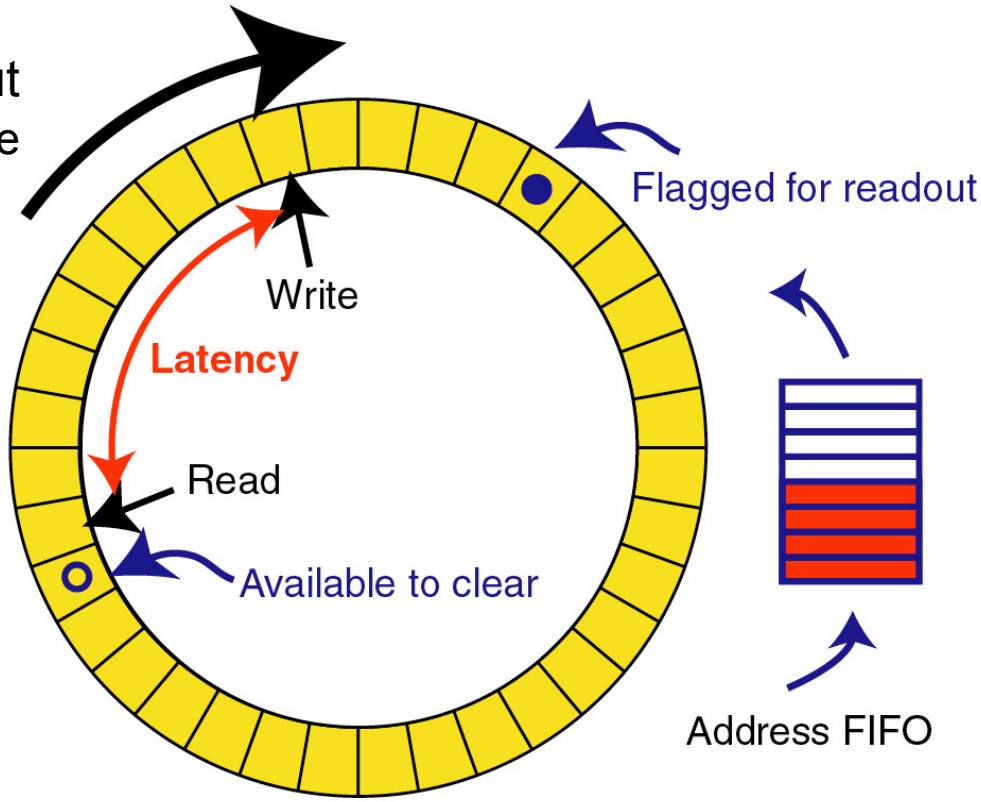
CMS Pixel module



ATLAS Liquid Argon Electromagnetic calorimeter

Front end memory

- Many detectors require on-chip buffering of data while awaiting readout
  - Multiple triggers possible and “deadtime free” storage desirable
- Data stored in pipeline memory with “ring” topology
- Pointers record current (write) location and location of data being read
- Addresses of used locations stored in FIFO to be skipped during writing
  - pipeline length is dynamic
- Pipeline length, buffer depth, storage time chosen to ensure that rate of data lost is sufficiently small
  - queuing problem



Noise in amplifier systems

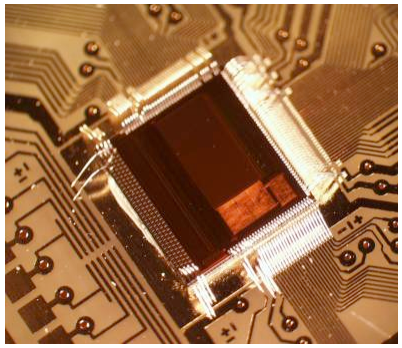
- VFE systems comprise
  - preamplifier - with noise sources and shaping amplifier or other filter
- Preamplifier usually designed with noise as an important consideration
  - preamplifier pulse shape is long duration, so modify it with shaper to
    - optimise signal to noise
    - generate a more practical pulse shape, avoiding pile-up

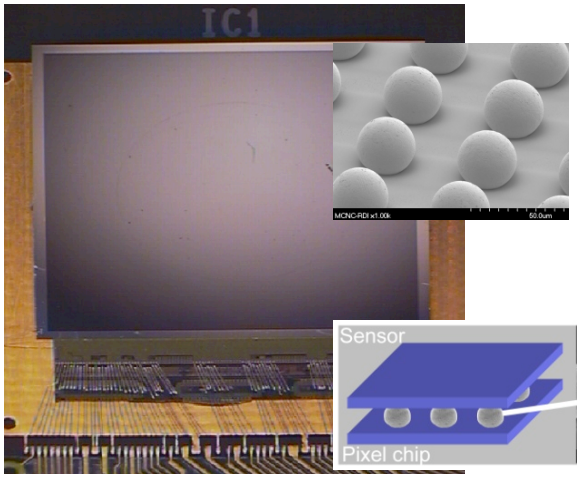
Intrinsic noise sources:

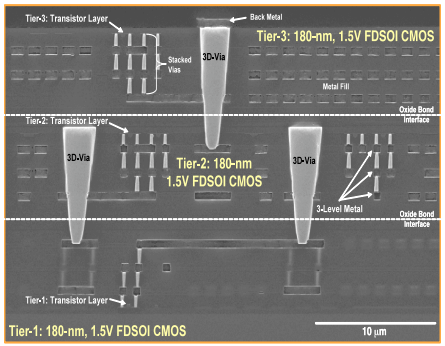
- Thermal noise
  - Quantum-statistical phenomenon; carriers in constant thermal motion
  - Typically associated with input transistor or resistive components
- Shot noise
  - Random fluctuations in DC current flow
  - Carrier transportation across semiconductor junctions (diodes and bipolar transistors).
  - Typically associated with sensor
- *1/f* noise
  - commonly present in MOS devices
  - Constant noise power in each decade 1-10, 10-100, 100-1000,
  - Luckily, less important for high speed electronics as needed at LHC

Connection to detector

- Discrete (Detector itself may be made from PCB)
  - Calorimeters, drift tubes, wire chambers, etc.
- Wire bond (silicon strips)
  - Use of multi level wire bonding have reached its limits
- Bump bonding (pixels)
  - Pixel chip and pixel detector bump bonded to each other
  - Fine pitch bump bonding not really yet standard industrial process so yield problems and delays are often encountered
- MAPS
  - Use electronics chip substrate as detector
  - Substrate may not be perfect for detector purposes. (leakage, charge collection, etc.)
  - Biasing and connection to detector part not obvious
- 3D: Our dream for the future
  - Multi level electronics and dedicated detector substrate in a chip stack
  - In R&D phase in several labs and companies
  - Will it offer sufficient yield and low cost for it to become available to us and others
    (consumer applications will determine its future or it may stay too expensive for us)
- Electronics is getting more and more integrated with detector itself (may even be on same silicon substrate)

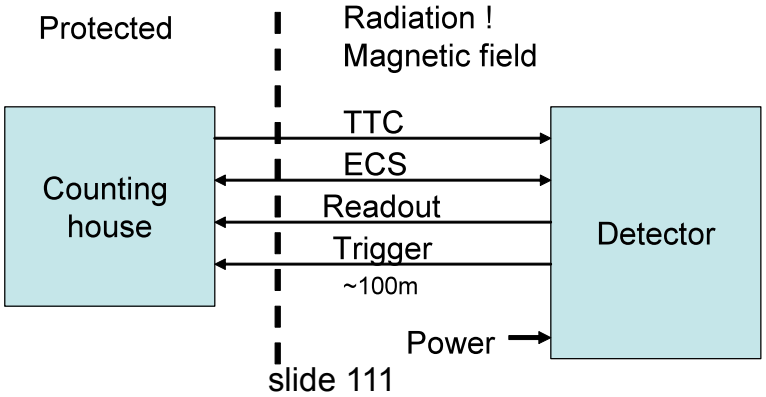






Connections to detector

- Timing Trigger Control (TTC) of front-end
  - Synchronize all detector channels to particle collisions and between channels to correlate hits from same event (not mixing events)
  - Trigger decisions to all pipeline buffers.
  - Speed and time precision determined by accelerator and specific requirements of detector (e.g. high resolution calorimeters)
- Control and monitoring: ECS=Experiment Control System or DCS= Detector Control System, Slow control
  - Read and write control and monitoring front-end registers
- Readout
  - Sending collected information from detector to DAQ interface
- Trigger
  - Sending high speed low latency information to trigger system (similar to readout links)
- Power
  - Obviously a very different connection type (see later)
- On-detector side may have significant radiation levels that prevent existing commercial solutions to be used (LHC).

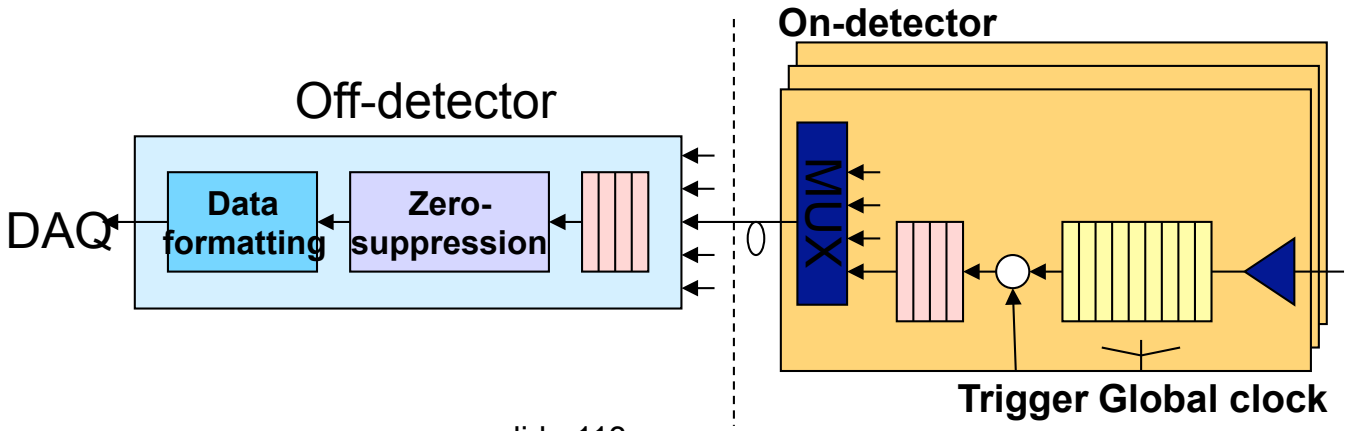


Readout architectures

- After basic analog amplification and shaping the architecture of the remaining front-end readout systems depends on many factors
  - Number of channels and channel density
  - Collision rate and channel occupancies
  - Triggering: levels, latencies, rates
  - Available technology and cost
  - What you do in custom made electronics and what you do in CPU farm based DAQ system
  - Radiation levels
  - Power consumption and related cooling
  - Location of digitization
  - Given detector technology
- All sub-detectors in an experiment MUST comply to one common basic architecture and some key parameters
  - There are lots of different good ideas of what is the best architecture and what suits my “private” sub-detector best.
  - Simplicity for large complicated systems for sure makes the difference between a good working experiment and a nightmare
  - A globally defined architecture can be implemented in many different ways

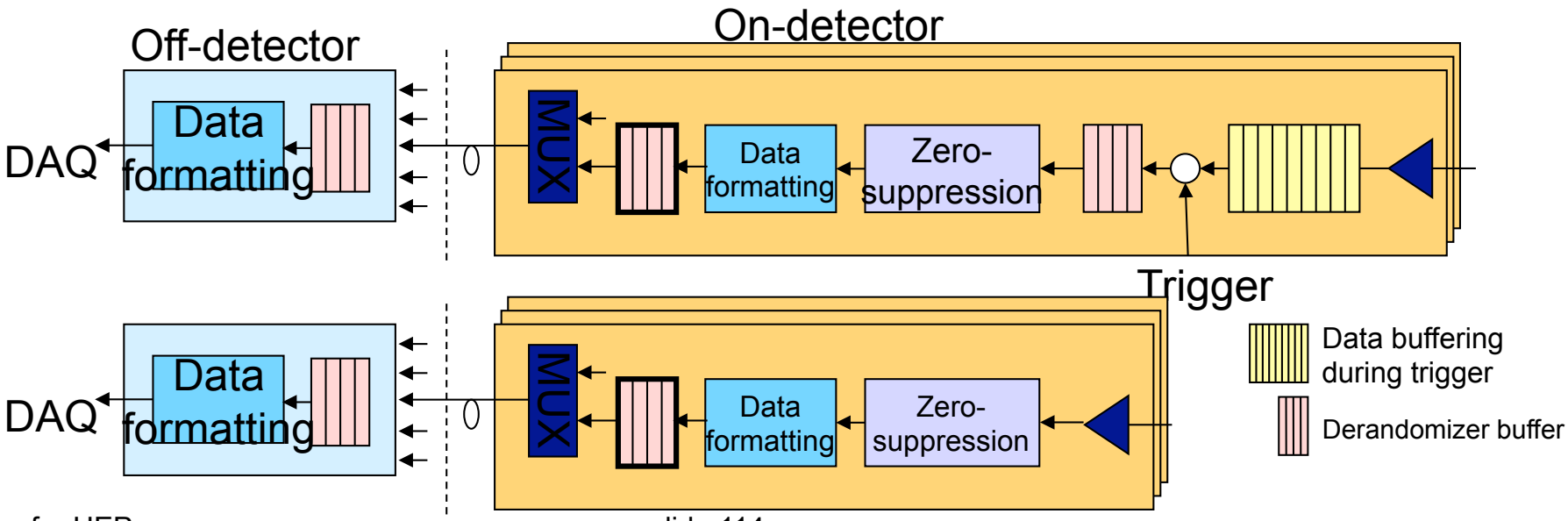
Synchronous readout

- All channels are doing the same "thing" at the same time
- Synchronous to a global clock (bunch crossing clock)
- Data bandwidth is "constant" (depends on trigger rate only)
- Data from all channels readout which allows DAQ system to perform common mode compensation and alike
- Buffers (de-randomizers) in the front-ends runs synchronous and can be prevented to overflow with a single central control
- Lots of bandwidth wasted for zero's
  - Price of links determine if one can afford this
- No problems if occupancy of detectors higher than expected
  - But there are other problems related to this: spill over, saturation of detector, etc.



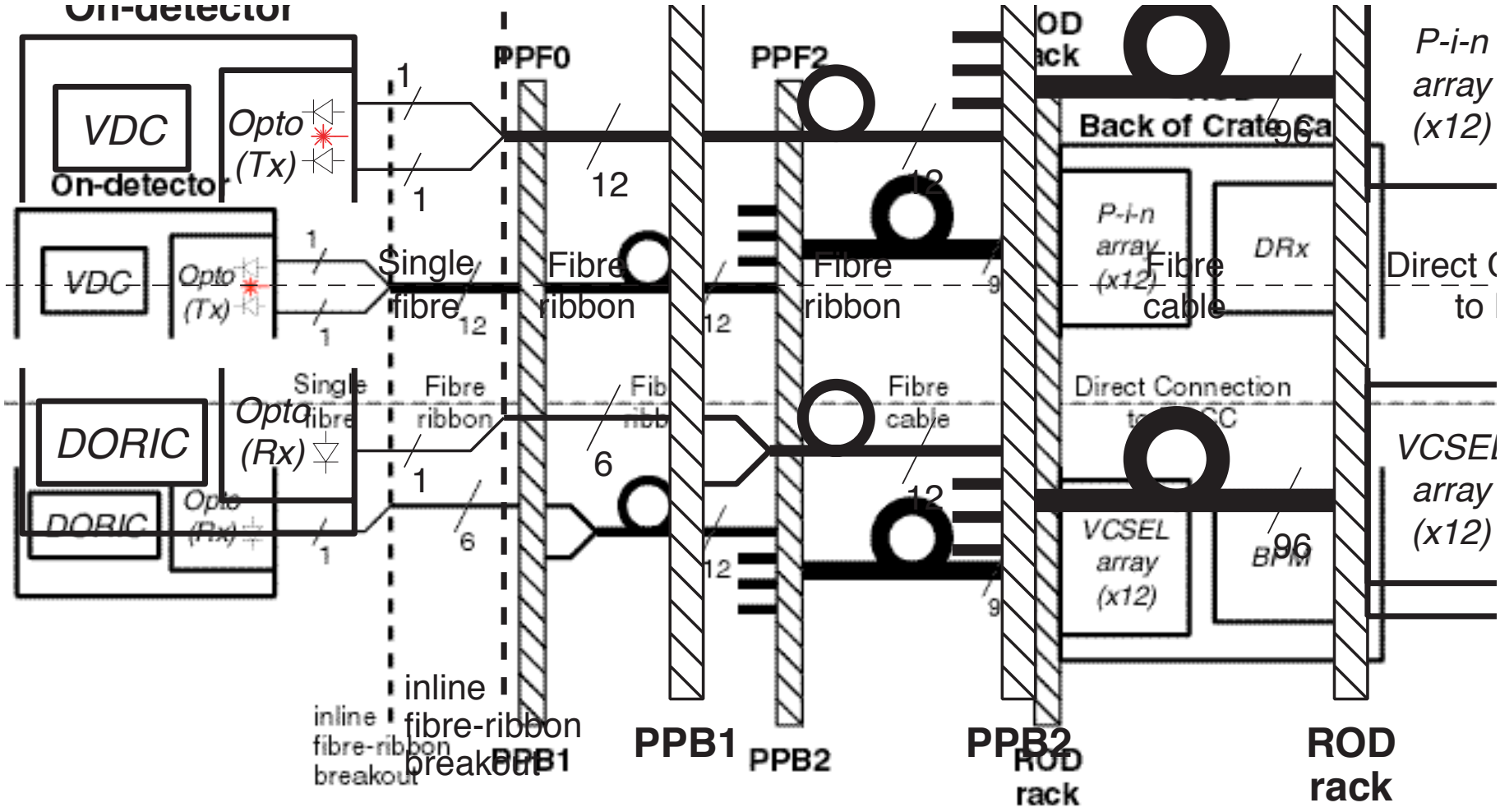
Asynchronous readout

- Only readout of non zero data
- Lower average bandwidth needed for readout links
  - Especially interesting for low occupancy detectors
- Each channel "lives a life of its own" with unpredictable buffer occupancies
- It is unknown if collected event actually contains all hits (unless running at very low trigger rate)
  - Or having a complicated scheme to keep track of what has been lost when a local data buffer has overflowed.
  - Detectors themselves do not have 100% detection efficiency either.
- Requires sufficiently large local buffers to assure that data is not lost too often
  - Channel occupancies can be quite non uniform across a detector with same front-end electronics
  - Efficient for detectors with low occupancies
- (may still use a global synchronous clock but is not synchronous at the event level)
- DAQ systems runs with zero-suppressed data but has very large buffers, lower rates and much more intelligence to handle this
- Async. readout of detectors in LHC: ATLAS and CMS muon drift tube detectors, ATLAS and CMS pixel detectors, ATLAS SCT, several ALICE detectors as relatively low trigger rate (few kHz).

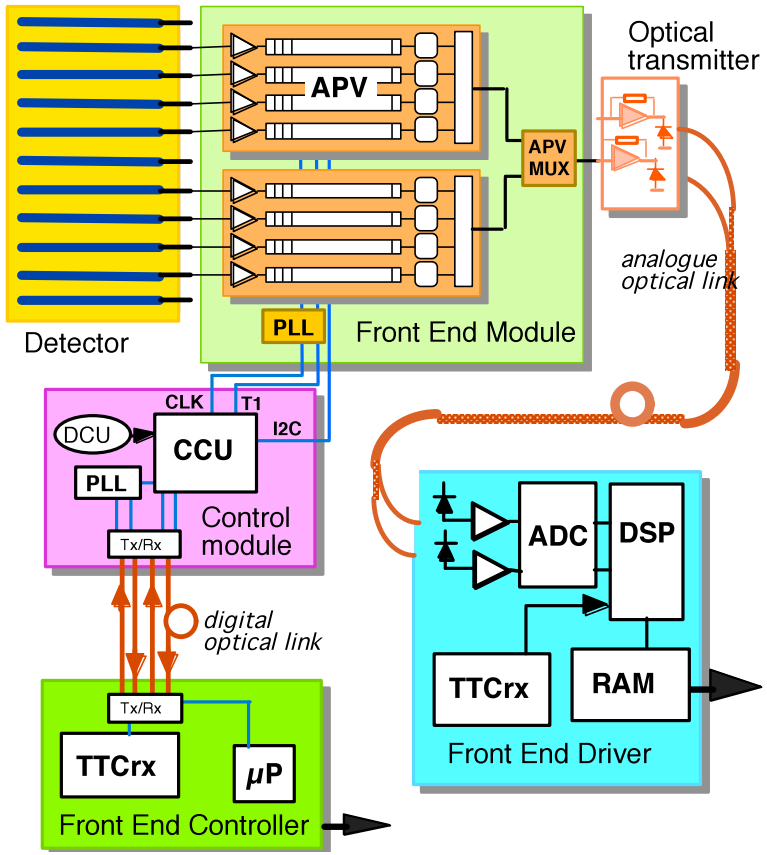


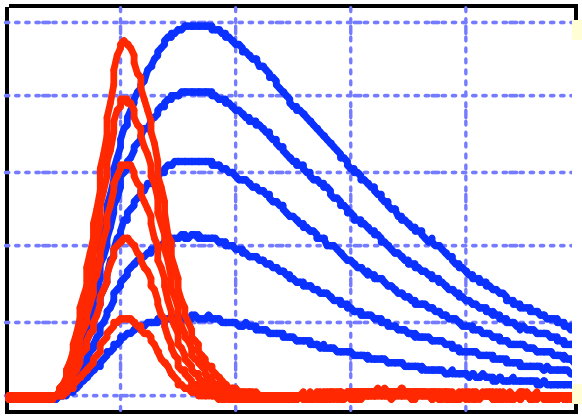
ATLAS SCT optolinks

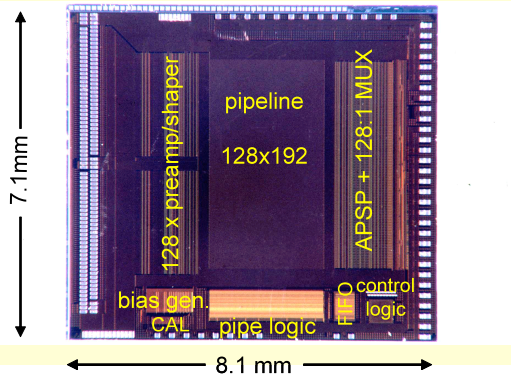
- VCSELs (850nm) + Si PIN diodes & multimode fibres

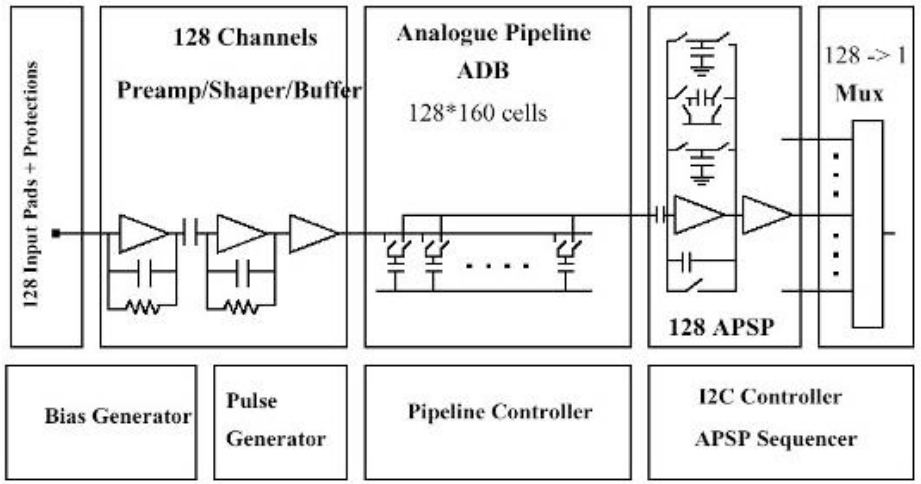


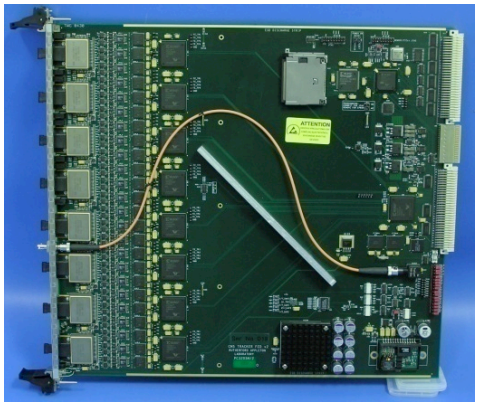
CMS

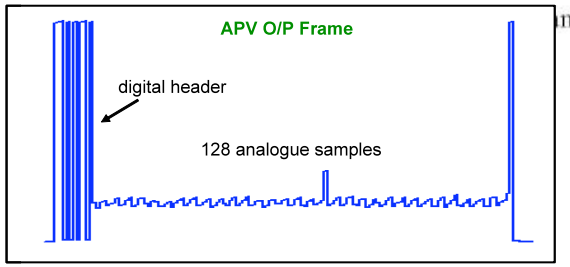

Optical transmitter
APV
APV MUX
analogue optical link
Detector
PLL
Front End Module
CLK
T1
I2C
DCU
CCU
PLL
Control module
Tx/Rx
digital optical link
ADC
DSP
TTCrx
RAM
Front End Driver
Tx/Rx
TTCrx
µP
Front End Controller




7.1mm
pipeline
128x192
128-x preamp/shaper
APSP + 128:1 MUX
bias gen.
CAL
pipe logic
FIFO control logic
8.1 mm

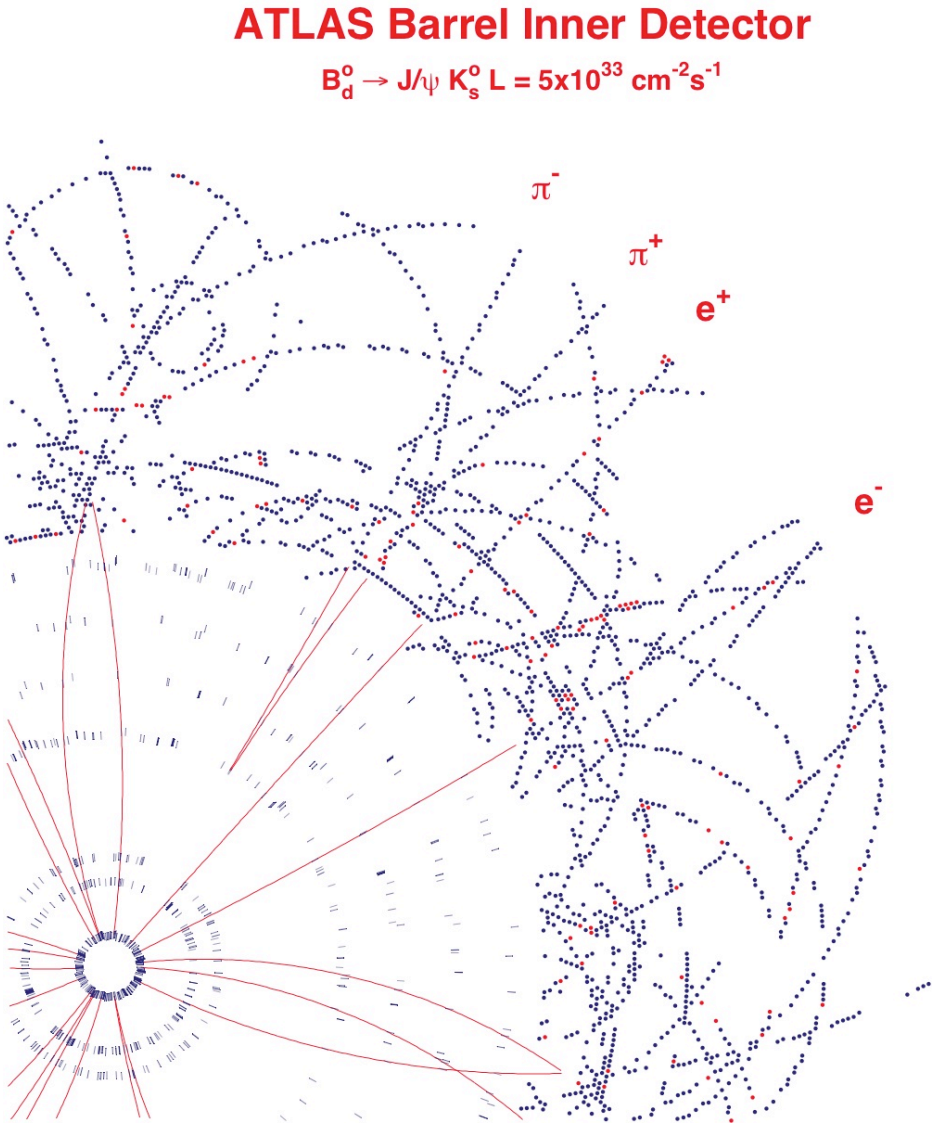

128 Input Pads + Protections
128 Channels
Preamp/Shaper/Buffer
Analogue Pipeline
ADB
128*160 cells
128 APSP
128 -> 1
Mux
Bias Generator
Pulse Generator
Pipeline Controller
I2C Controller
APSP Sequencer




APV O/P Frame
digital header
128 analogue samples

Main detector requirements..

- for colliding beam and fixed target experiments:
  - Magnetic field to bend trajectories
  - Material - enough to generate signals but minimise scattering, secondary interactions, conversions,…
  - Enough layers - to recognise trajectories easily and reconstruct them reliably
  - Large numbers of sensor channels to easily distinguish tracks and achieve required spatial resolution
  - Best spatial precision near the interaction point
- Generally can't ignore cost

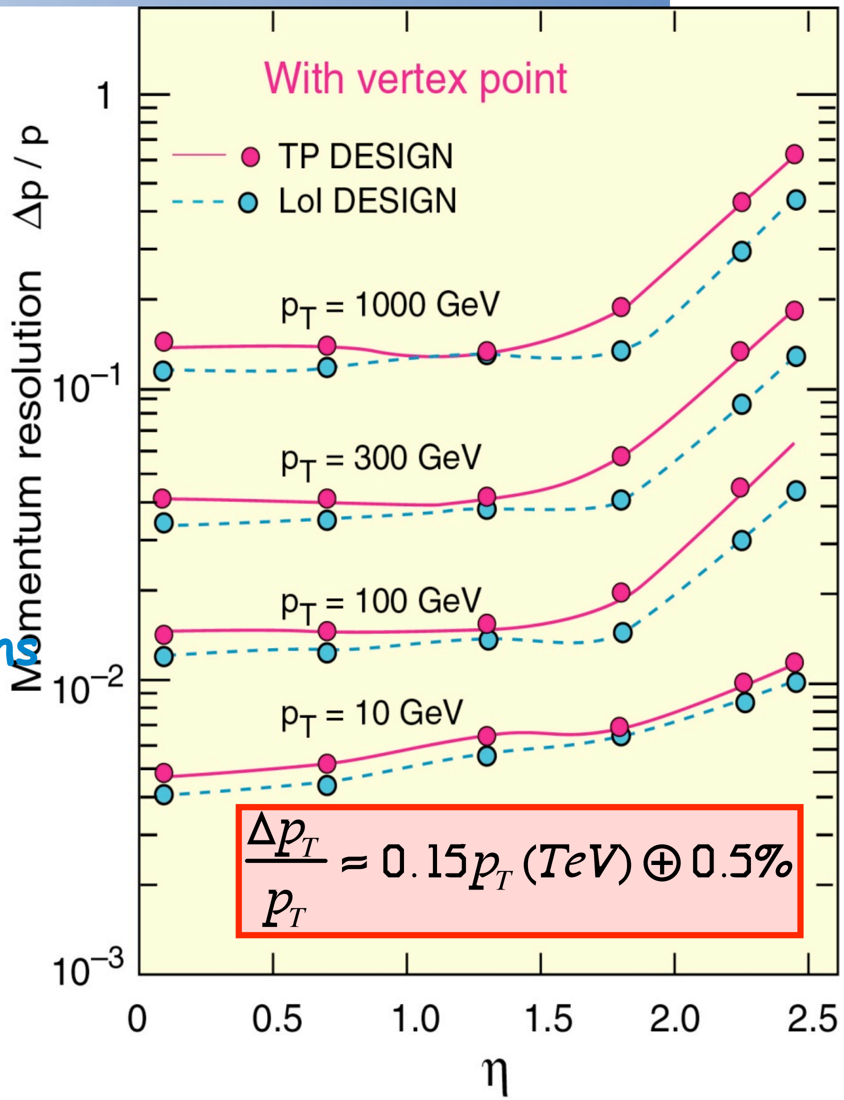


Quantitative requirements

- p resolution

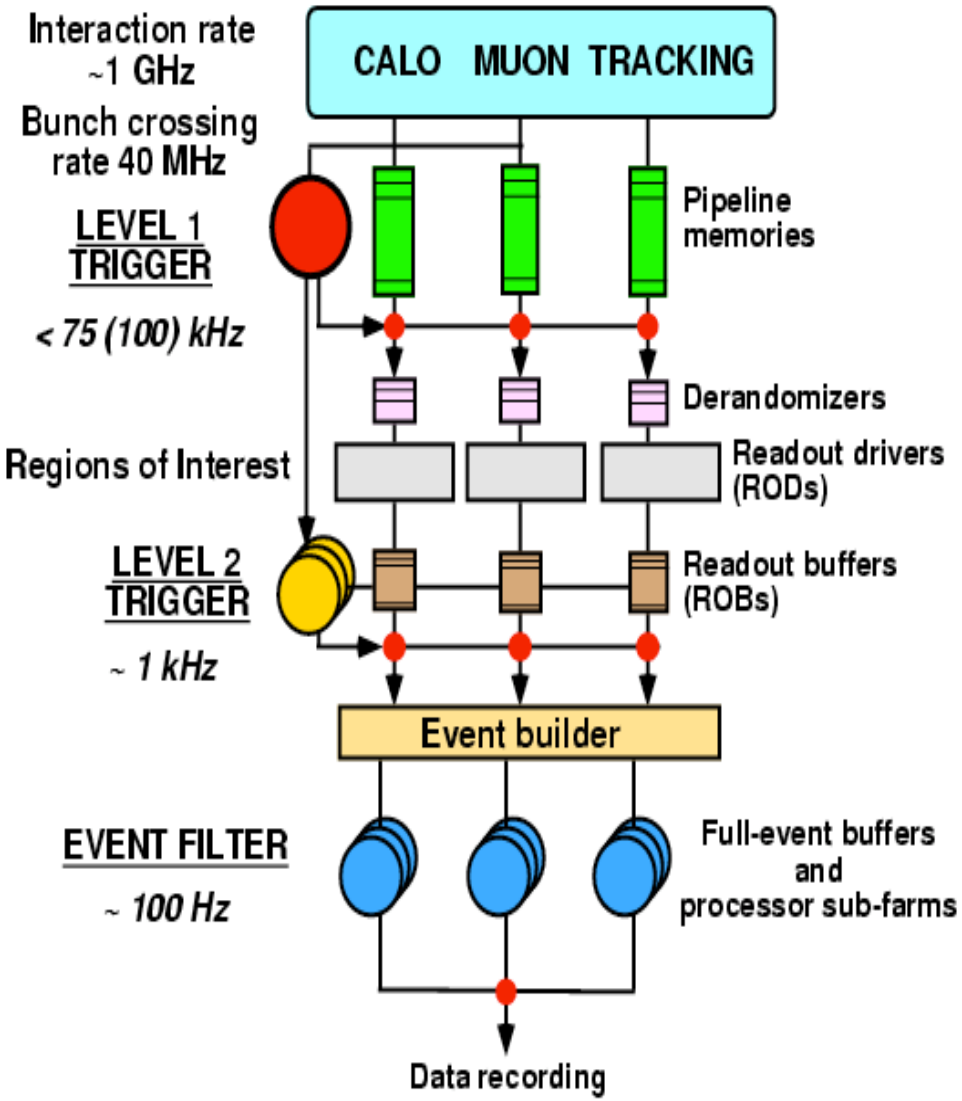
$$\frac{\sigma(p_T)}{p_T} \sim p_T \frac{\sigma_{meas}}{B.L^2\sqrt{N_{pts}}}$$

  - maximise B, L, N_{pts}
  - high precision space points
- minimise multiple scattering
  - and bremsstrahlung, photon conversions
  - Low Z materials desirable
- well separated particles
  - Not only low occupancy…
  - so high granularity, but also…
  - …adequate time resolution



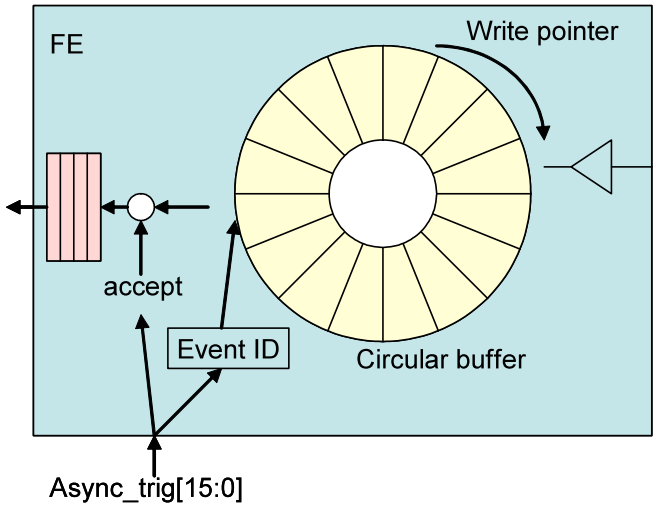
Typical LHC read out

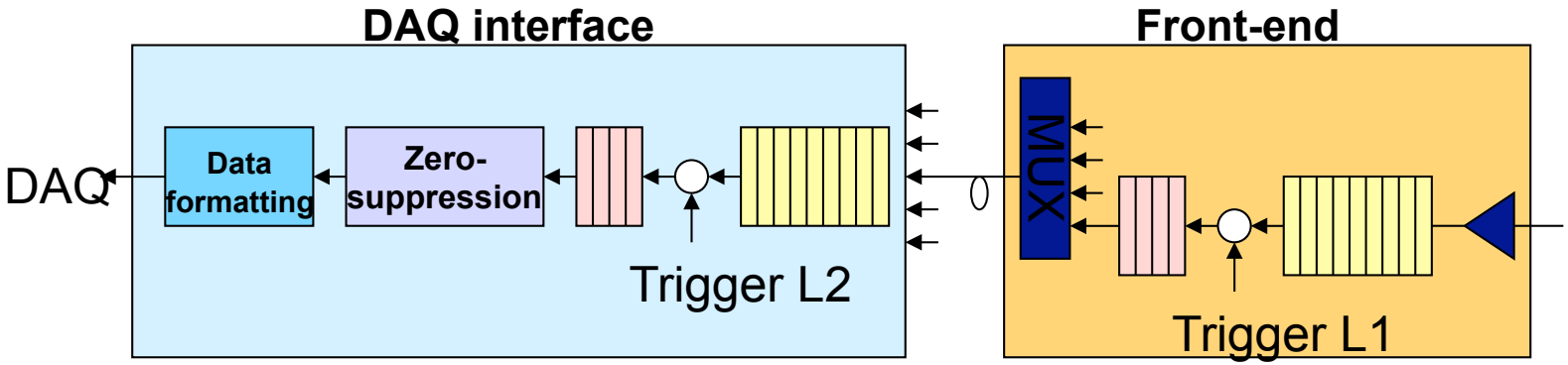
- 40MHz sampling rate
- Triggered at few kHz - 1MHz rate
- Constant latency buffer of a few μs (few hundred samples at 40MHz)
- On-detector:
  - Analog front-end
  - Extraction of data for trigger
  - Latency buffer
  - Readout via optical links (many)
  - Timing and trigger control
  - Controls and monitor interface
  - Difficulties: radiation, space, cooling, access, magnetic fields
- Off-detector:
  - Trigger systems
  - DAQ interface
  - Global readout and trigger control
- Digitization: **on-detector** or off-detector



Multilevel triggering

- First level triggering.
  - Hardwired trigger system to make trigger decision with short latency.
  - Constant latency buffers in the front-ends
- Second level triggering in DAQ interface
  - Processor based (standard CPU's or dedicated custom/ DSP/FPGA processing)
  - FIFO buffers with each event getting accept/reject in sequential order
  - Circular buffer using event ID to extracted accepted events
    - Non accepted events stays and gets overwritten by new events
- High level triggering in the DAQ systems made with farms of CPU's: hundreds – thousands.
  (separate lectures on this)





Future power problems

- For future front-end electronics based on new deep sub-micro technologies the power per function is clearly decreasing
  - Not always the case for the analog part
  - We will put in more channels and more functions
  - Uses lower power supply voltage (e.g. 1.2 v instead of 2.5v)
- If we in the end need the same power the required current will become ~2 times larger which implies that our cable losses will get ~2 times worse.
- So thicker cables and more cooling needed: DOES NOT LOOK LIKE A GOOD IDEA

What is the solution ?

- **Consume less power (but not so easy)**
- **Use of local DC-DC converters at the loads**
  - Radiation, magnetic fields
  - Switched capacitor converters
    - Unconventional, limited voltage ratio
  - Use of air core inductor converter
    - Efficiency ?, EMC noise ?
  - Use of ceramic transformers ?
    - Not a well known and mature technology
- **Serial powering**
  - Grounding, failure modes ?, noise coupling ?