PCB design guidelines for chip on board (COB) applications

Prepared by the Die Products Consortium (DPC)

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1. Objective

This document provides guidelines to designers of printed circuit boards (PCBs) who are converting surface mounted packaged ICs to include a bare die implementation. The first assumption is that this conversion is being done primarily for cost savings – that is, the total cost for an assembled board using some bare die will be less than the cost for the assembled board using traditional surface mount components only. Fabrication of the PCB using the largest possible "minimum" feature size will ensure that the yields are as high as practicable. The footprint of the die on the board is the area where these minimum feature sizes may be required, so this document will focus on layout requirements of the substrate for COB assembly.

The National Technology Roadmap for Electronic Interconnections[1] projects that PCBs for low cost consumer products will require 150/150 μm lines and spaces, at least 2 layers, with minimum diameter through-via of 350 μm, with a land diameter of 400 μm surrounding the hole. These requirements are well within the capabilities of board fabricators using conventional technology today.

2. Methodology

This guideline uses models of two ICs to develop a basic understanding of the issues related to moving from a surface mount technology (SMT) PCB design to a COB PCB design. However, it is imperative for a PCB designer to obtain the exact layout design rules from both the board fabricator and the board assembler to ensure satisfactory yields.

3. Chip on Board

The most readily available form of die products are termed bare die. These die are identical to the die that are used in the vast majority of single chip packages today as they are wire bonded to a lead frame or interconnecting substrate. The use of wire bonded die mounted directly to the PCB is termed chip-on-board, (COB). COB is the most mature and largest part of the bare die market. Chip on board technology is characterized by the following factors:

- Bare die are mounted directly on an interconnecting substrate or PCB, along with other packaged die, discretes and/or passive devices.
- Die are mechanically attached to the substrate using conductive or non-conductive epoxies
- Die are electrically connected to the substrate using wire bonding
- Die are encapsulated with a protective shell

For low-cost Chip-on-Board (COB) technology, the substrate usually used is FR-4 material (glass fiber reinforced epoxy) due to its low cost. Electroless nickel/gold is recommended for the metallization because it completely covers the top surface and side

walls of a metal pad and supports various electrical interconnection methods[2] as may be required for a mixed SMT/COB application.

The most popular low cost chip to board electrical interconnection methodology for bare die in use today is wirebonding. This implementation utilizes standard bond pad metalization and surface passivation on the IC. The chip I/O are located on the periphery of the device. Exact location and size of the bondable surface along with the surface metallurgy are defined on the Die Product datasheet from the IC supplier. Bonding technologies for COB interconnects include thermosonic bonding (gold-ball bonding) at elevated temperatures and ultrasonic bonding (aluminum wedge bonding) done at room temperature.

Gold-ball bonding is a high throughput, high strength technology that allows for bonding of fine pitch bond pads. It requires an elevated temperature to make reliable bonds. Process consideration must be given to the set up conditions, wire diameter, wire length, metallurgy and surface conditions.

Aluminum wedge bonding can be processed at room temperature and utilizes lower cost wire. Lower bond strength and lower throughput can be expected. Additional process consideration should be given to wire bond angles and forward/reverse bonding effects when using wedge bonding.[3]

It is important to consider the order of assembly when including wirebonding attachment methods with surface mount technology that makes electrical connections by reflowing solder. The preferred method of assembly is to assemble and reflow the surface mount components prior to assembling and bonding the COB devices.[4] Note that the height of the surface mount components may interfere with the wire bonding operation if they are placed too close to a bare die. Usually, a spacing equal to 2X the height should be provided. The PCB designer should check the design rules that will be used during the assembly process.

3.1. Substrate

Substrate technology for low-cost board assembly is almost exclusively epoxy-glass laminate, such as FR4, which is the material of choice for surface mounted ICs as well as bare die mounting. There are tradeoffs for implementing chip on board substrates in terms of substrate materials, board finish, etc, which should have been made prior to the layout decisions outlined in this document.

3.2. Layout

The diameter of the gold wire used in ball bonding ranges between 20 μm and 33 μm. The corresponding ball diameters are typically between 2.5 to 5 times the wire diameter[5], but may range from 1.5 times for small ball applications with fine pitches, to 3 to 4 times for large bond pad application.

A “footprint” of the bond fingers is fabricated as lands on the substrate, just outside die edges, and interconnected to the circuit traces on the substrate. See figure 1.

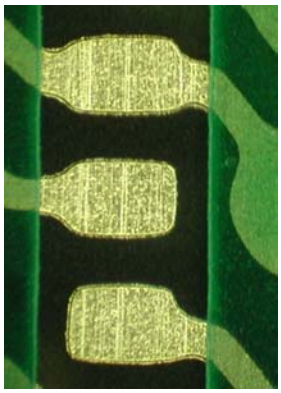


Figure 1: Three bond fingers on a substrate, with interconnections to other circuitry on the substrate. Note that the bonding area is not over-coated with solder mask.

Power and ground rings may be included in the footprint. Figure 2 shows the relationship of the footprint to the die, and includes both a ground ring and a power ring. There may be several rings as required by the die. Except for the respective power and ground wire bonding sites, these rings should be covered by the solder mask to prevent contacting of sagging bond wires to the ring[6] , which could result in a short circuit.

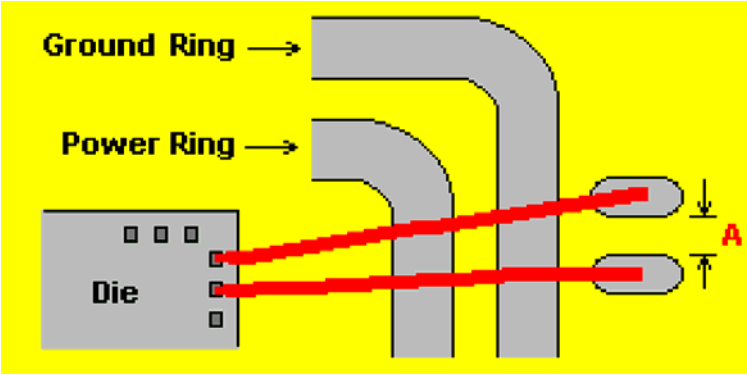


Figure 2: Bonding wire extends from I/O pad on die to interconnecting pad on substrate. The substrate bond fingers are aligned in a one to one ratio with the signal I/O pads on the die, assuming power and ground pads are connected to the rings only. The substrate footprint pads must follow the design rules for the lines and spaces on the PCB. Power and ground rings may be added within the substrate bonding pad ring.
Drawing source: Cadence Design Systems

Figure 3: Photo showing chip (on left) and wires connecting to bond fingers on substrate (right side of picture.) Photo by HKPC, courtesy of National Semiconductor.

3.3. Bondfingers

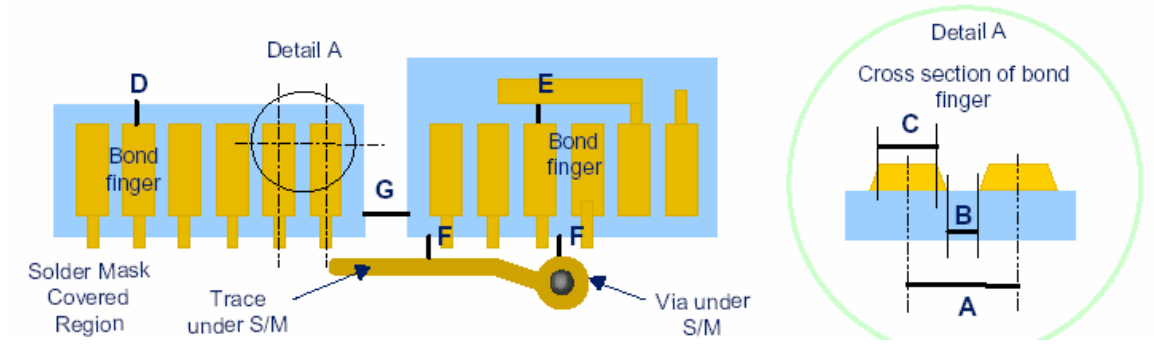


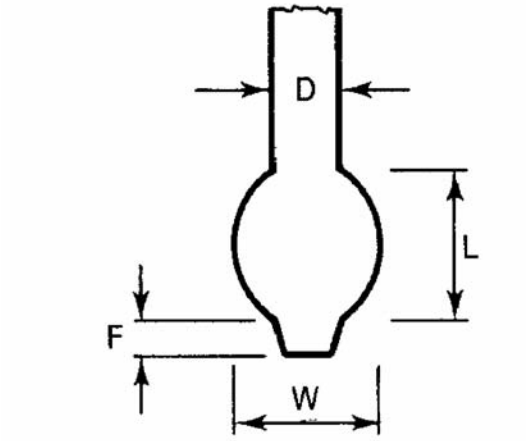
Figure 4: Bond Finger Design rule layout showing critical dimensions. Typical bondfinger length is 0.6 - 0.8 mm[7].
Drawing source: Infineon.

	Design Feature
A	Bond finger pitch
B	Bond finger space
C	Bond finger width
D	Solder mask clearance for bond finger
E	Min. bond finger to trace space
F	Min. Solder Mask extension to tract/via land
G	Min. solder dam width

Table 1: Nomenclature for figure 4.

The bondfinger size should accommodate the bond size of a typical wedge or crescent bond plus bonding tool accuracy as worst case. A typical wedge bond is shown schematically in figure 5. For example, if the wire diameter is 25 µm, the maximum bond width would be less than 62.5 µm, and the maximum bond length will be less than 125 µm. The assembly foundries may offer tighter design rules. They should be consulted

first. In reality, it is good practice to make the bond fingers long enough to accommodate several bond sites, so that any rework of the site can be done on clean, bondable surfaces. The pad's long axis should be oriented along the intended wire path for a wedge bond.



D = Wire Diameter

L = Bond Length

$1.5D \leq L \leq 5.0D$

W = Bond Width

$1.2D \leq W \leq 2.5D$

Figure 5: Outline view of an aluminum wedge bond showing allowable[8] dimensions of the wedge. These dimensions provide a "rule of thumb" for the minimum size of the bonding pad for ultrasonic bonding of aluminum wire on the PCB. Note, however, that advances in ultrasonic systems have made it possible to produce a high-strength wedge bond that is only 2-3μm wider than the wire diameter, resulting in finer pitch capabilities.

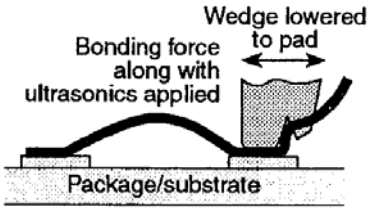
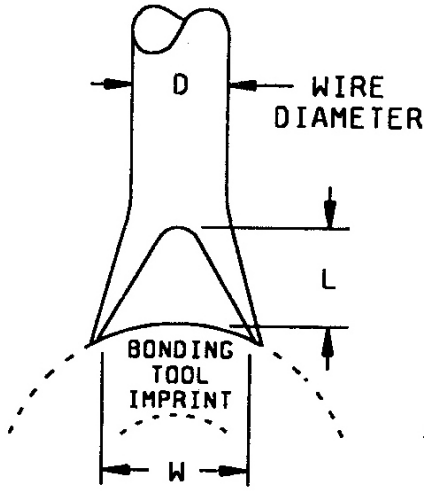


Figure 6: Drawing[9] showing wedge bonding operation on the second bond, at the substrate bond finger.



D = Wire Diameter

L = Bond Length

$0.5D \leq L \leq 3.0D$

W = Bond Width

$1.2D \leq W \leq 5D$

Figure 7: Tail or crescent bond is the shape of the thermosonic bond on the substrate (ball bond is on the die side). The allowable[10] dimensions are shown in the box to the right of the figure. Again, these dimensions provide a guideline for the minimum size of the bonding pad for thermosonic bonding of gold wire on the PCB.

The size and shape of the crescent bond (tail of a thermosonic bond) are directly related to the diameter of the wire and the geometry of the capillary. Because of shrinking silicon and finer wirebond pitch (which requires smaller and smaller capillary on the bonding tool); it is imperative to have adequate face dimension between the edge and capillary of the bond tool for high reliability bonds. See the outline of the bonding tool imprint in figure 7.

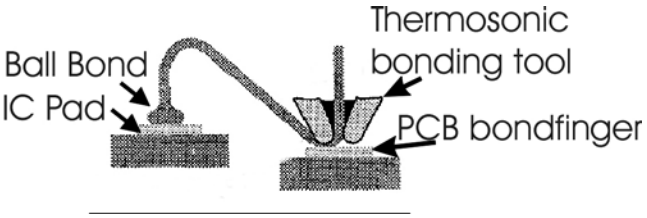


Figure 8: Drawing[11] showing one complete thermosonic bond. The wire is threaded through the capillary within the bonding tool and the tool tip from the capillary to the outer edge is applied to make the tail (or crescent) bond (see figure 5).

3.4. Bondfinger pitch

The distance between bondfingers should be large enough to avoid shorting between adjacent wires. The wirelength should be less than 5 mm long to prevent excessive sag and "sweep". In practice, an aspect ratio of 100D maximum (D is the diameter of the wire) is a good design guideline for obtaining high manufacturing yield.[12]

Bond wire length is the limiting factor in the space transformation between die and substrate. Figure 9 shows the relationship between the die size and footprint size for differing lengths of bond wires.

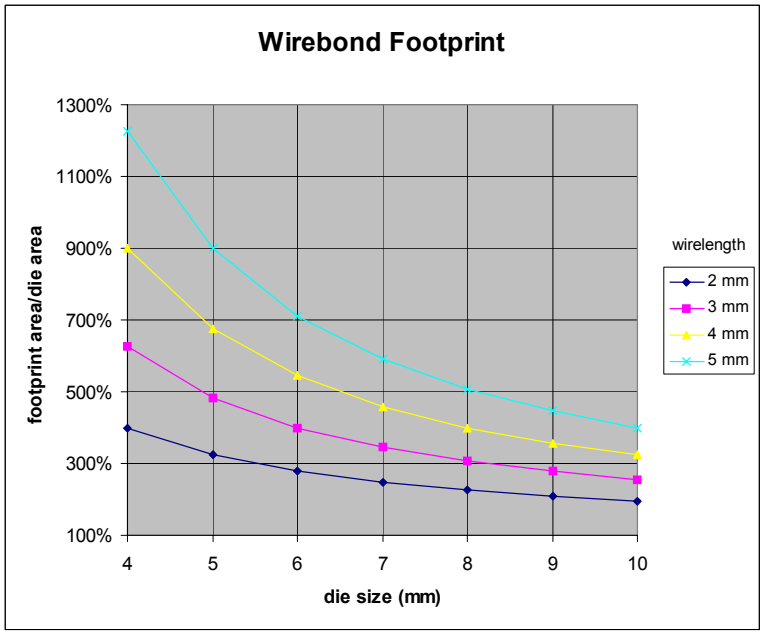


Figure 9: Wirebond footprint area is a function of bond wire length. The maximum length of the wire is limited by the sag and "sweep" of the wire. These are a function of the length and diameter of the bonding wire.

To obtain high yielding PCBs, the bondfinger size and pitch must fall within the PCB fabricator's standard design rules. If the pitch of the die is finer than that supported by the PCB design rules, the bond finger pads can be placed radially on the substrate so the PCB pitch will fan out from the center of each side[13].The tradeoff for increasing the footprint-area to die-area ratio is the bond-wire-length impact on the yield of the assembled PCB. See figure 10. See appendix A for the bond length calculation[14].

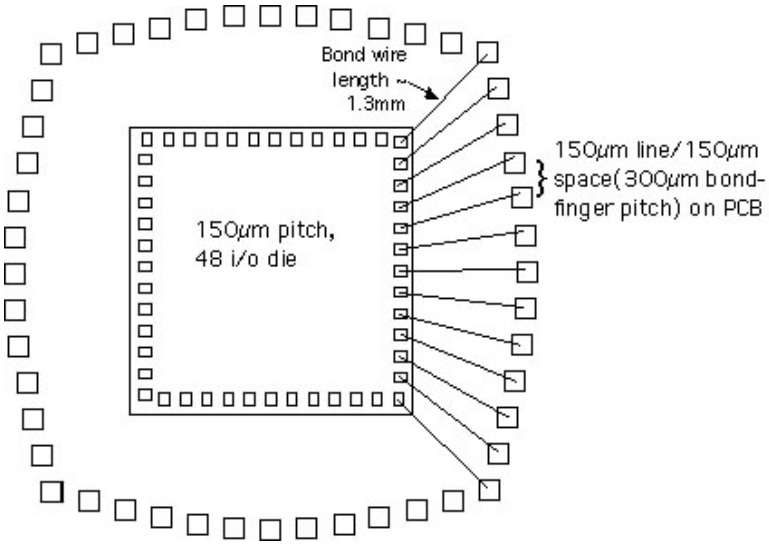


Figure 10: Drawing of 150µm pitch die with fanout to 300µm pitch bondfinger on the PCB. The drawing shows only one side of the wirebonds in place. The 300µm pitch on the PCB allows the design to stay above the minimum line and space fabrication design rules for low cost PCBs. Assuming a wire diameter of 25µm, the wire length is also well within the optimum length of 100 x diameter of the wire. Note that in this example, all bondwires are designed to be the same length. (The length is the projection of the bond wire onto the plane of the PCB surface).

Silicon shrinkage and fine pitch on the die may increase the wire lengths significantly[15]. See figure 11.

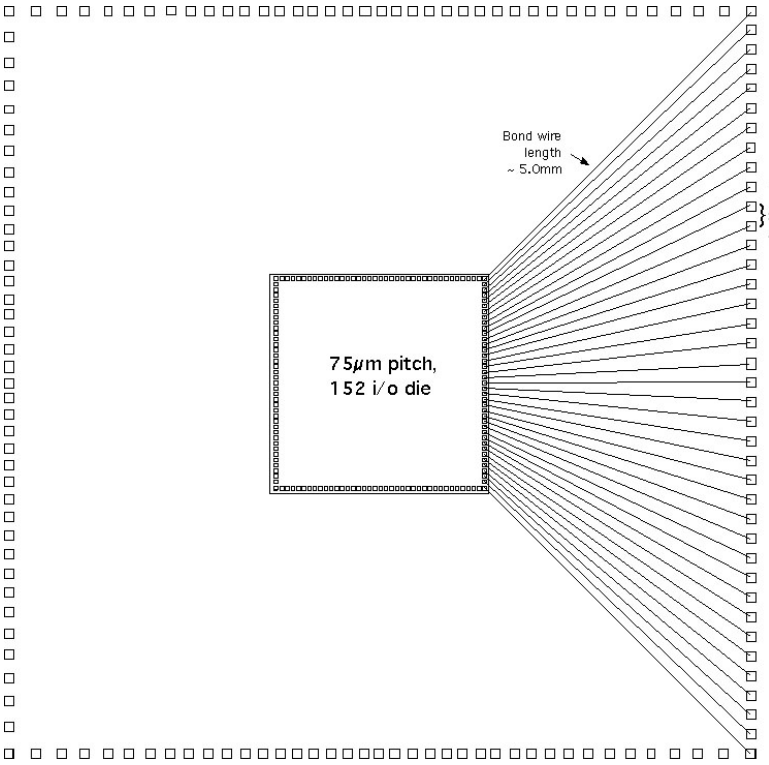


Figure 11: A die with very challenging feature sizes may still be accommodated by wirebonding on conventional PCBs. Up to 5mm wire length is needed at the corners to allow the space transformation of the fine pitch on die to the larger pitch on the board. 125µm line/125µm space design rules are becoming typical for low cost consumer PCB technology.[1]

Figure 12 shows the options discussed in Figures 10 and 11.

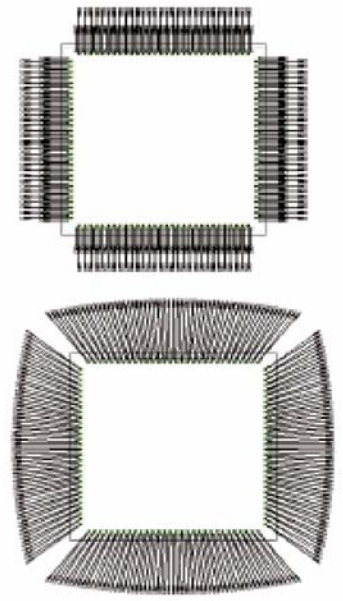


Figure 12: Top drawing shows bondfinger pad layout orthogonally from die pads, at the same pitch. The bottom drawing shows bondfinger pads arrayed radially from die pads, resulting in relaxed pitch requirement for the PCB pads.

Drawing source: CAD Design Software: Hybrid/MCM Designer Suite

If the bond wire length must be larger than 5 mm in order to accommodate the minimum line and space design rule for the bond finger fabrication, the designer may use a dual row of bond fingers. See figure 13.

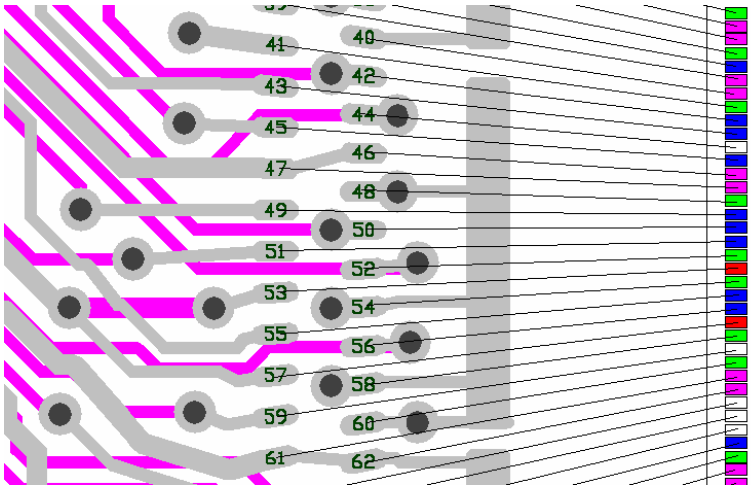


Figure 13: This figure shows a staggered bond finger layout that routes the inner row (even pads 40 – 62) of bond finger pads down to an inner layer of the PCB or to a power/ground ring inside the bondfinger rows. This allows support for a die with tighter pitch while respecting relaxed board fabrication and assembly design rules, as well as minimizing the board area required for the device. Source: PWB Design Guidelines Tutorial, 10th Annual KGD Packaging and Test Workshop.

4. Diebonding

The die is bonded to the PCB using a die attach epoxy. A good die attachment is made when a fillet is allowed on the perimeter of the gold plated die attach pad. The suggested[16] perimeter is found in table 1.

	Suggested perimeter	
Relative die size	**Longest die side**	**Adder per side**
Small	< 3mm	0.4mm
Medium	< 6mm	0.55mm
Large	>6mm	0.75mm

Table 1: Additional area under die to allow bleed-out of die-bonding adhesive.

If the die attach pad is metalized for electrical or thermal contact to the die, it should have a nickel barrier to protect the silicon from copper migration. The adhesive used to mount and hold the chip has silver or gold mixed with epoxy. This makes the adhesive both electrically and thermally conductive. The bottom of a chip is usually at ground potential and the die attach pad must therefore be connected to the circuit ground of the PCB[17]. If backside contact is not required for thermal or electrical conductivity, then the solder mask on the PCB will provide a planarized surface for a die attach pad.

In any case, the bond finger pads should be placed at least 0.4 – 0.75 mm away from the edge of the die attach pad to preclude shorting by the conductive die attach adhesive[18].

To reduce the difficulty in placing parts accurately, cameras are added to automatic equipment used in COB production. Optical patterns called fiducial marks are fabricated on the PCB and used by the camera to align the PCB for chip placement, test probe support, and automatic optical inspections. Fiducial mark designs should be coordinated

with vision system requirements, and should be placed on the substrate in the same process steps as the lands (the land is a portion of a conductive pattern usually used for the attachment of the component).

5. Encapsulation

Encapsulation is the process of providing a protective shell over the die. In most instances, the encapsulant is dispensed in a liquid, so provisions must be made in the board layout to allow sufficient space for the dispensing tool to operate around the perimeter of the die. See figure 14.

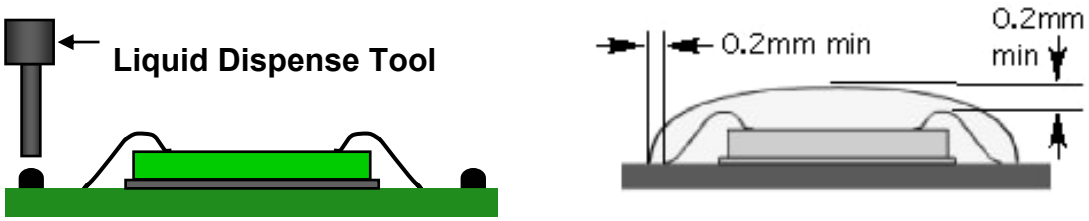
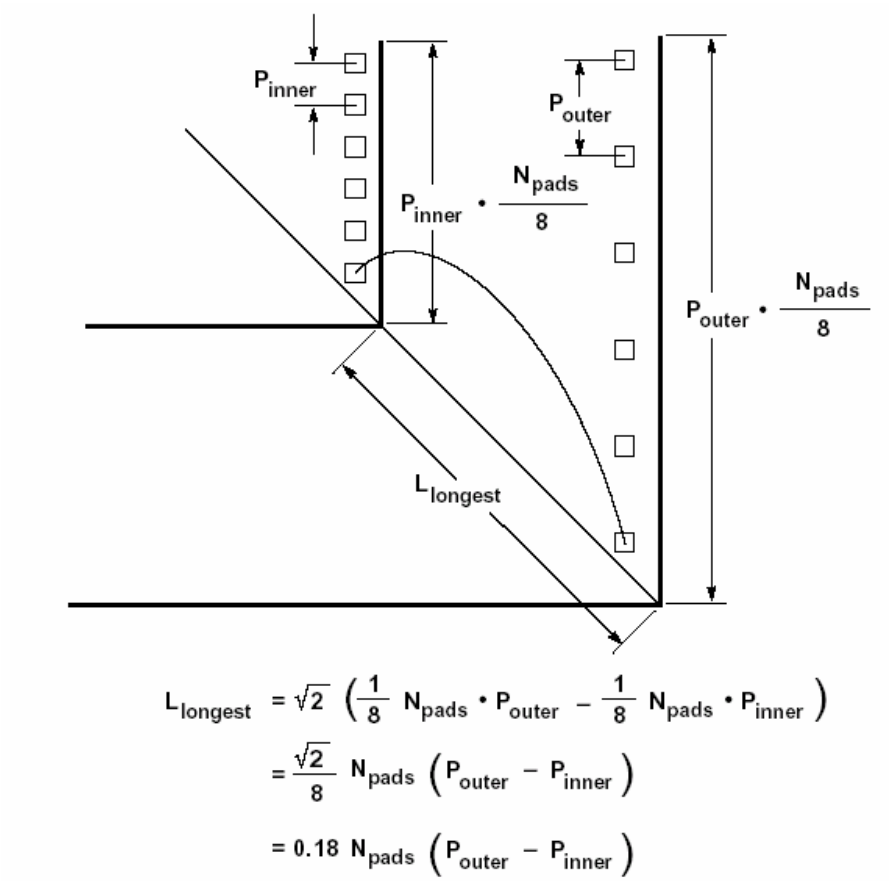


Figure 14: The encapsulation process may require space for the dispense tool to operate. The board assembly design rules will specify the "keep out" area, which will be outside of the bond sites on the PCB and not spread to touch adjacent components. The drawing on the right shows the typical encapsulation design guidelines[19]. Drawing source: National Semiconductor

Open vias should not be used in the encapsulation area of the COB design due to capillary wicking and leakage[20].

Appendix A

The calculation for the longest wirebond length, found at the corner of the die, is shown in the figure below.



$$L_{longest} = \sqrt{2}\left(\frac{1}{8} N_{pads} \cdot P_{outer} - \frac{1}{8} N_{pads} \cdot P_{inner}\right)$$

$$= \frac{\sqrt{2}}{8} N_{pads}\left(P_{outer} - P_{inner}\right)$$

$$= 0.18\, N_{pads}\left(P_{outer} - P_{inner}\right)$$

Figure A-1: Longest wirebond calculation[21]. In the figure above, L is the projection of the wire onto the horizontal surface of the PCB, N is the number of pads on the die, P_{outer} is the bond finger pitch on the PCB and P_{inner} is the bond pad pitch on the die.

Glossary

Adhesive – A substance such as glue or cement to fasten objects together. In PCBs, an epoxy adhesive is used to adhere components to the substrate.

Annular Ring – That portion of conductive material completely surrounding a hole.

Bare Die – An unpackaged discrete or integrated circuit. Bare die have bond pads on the upper surface suitable for interconnection to the substrate or package by wire bonding or soldered wiring.

Bondfinger – Land on PCB that is used as the site for the wirebond connection from the component. The number of bond fingers is equal to the number of connections that must be made from each component to the interconnecting substrate to form the circuit. The bondfinger layout on the PCB comprises the footprint.

Chip-on-board - Technology with which bare die are bonded to boards/substrates and wire bond connections are made from board to die.

Design rules – Sets of guidelines provided by the PCB fabricator and the PCB assembler that detail the geometry constraints for a particular board fabrication or assembly process.

Die bonding – Attaching of a semiconductor die to the package or substrate. Also called die attachment.

Electroless (deposition) – The depositing of a conductive material from an autocatalytic plating solution without the application of electrical current.

Encapsulation - Sealing or covering of a microcircuit to provide mechanical and environmental protection.

Fiducial marks – Features that are created in the same process as the conductive pattern and that provides a common measurable point for component mounting with respect to a land pattern.

Footprint – A combination of lands on a PCB that are used for the mounting, interconnection and testing of a particular component.

Interconnecting substrate - A base material and the metal layers which form connections for the electronic components that are attached.

I/O pads – the input and output connecting structures on a device.

Land (on PCB) – A portion of a conductive pattern used for the connection or interconnection of components on a printed circuit board (PCB).

Lead Frame – The metallic portion of a device package on which an integrated circuit die is mounted. Interconnecting wires connect the die bonding sites to the structure that becomes the outer leads of the package.

Pitch – The nominal center-to-center distance of adjacent conductors or I/O pads on a device.

Short Circuit – A fault that causes two or more points that are normally electrically separated to be connected.

Solder Mask (S/M) – A heat resisting coating material applies to selected areas on the surface of the PCB to prevent the deposition of solder on those areas during subsequent soldering.

Thermosonic bond – Terminations made by combining pressure and heat with ultrasonic energy to implement the join.

Through-via – A hole drilled through the PCB that is plated with conductive material to allow electrical connections between layers on the PCB.

Ultrasonic bonding – A termination process that uses ultrasonic-frequency vibration energy and pressure to make the join.

Wire sag – Failure of a wirebond wire to form the desired loop between its bonds.

Wire sweep – Movement of wirebond loops during transfer molding or encapsulation process.

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